

# Silicon photonics: a new technology platform to enable low cost and high performance photonics

L. Pavesi



UNIVERSITY OF TRENTO - Italy

**DEPARTMENT OF PHYSICS**  
**Nanoscience Laboratory**

# Outline

- Silicon Photonics
- State of the art
- Silicon Photonics for lab-on-a-chip
- NanoSilicon photonics
- Conclusion



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The experts look ahead

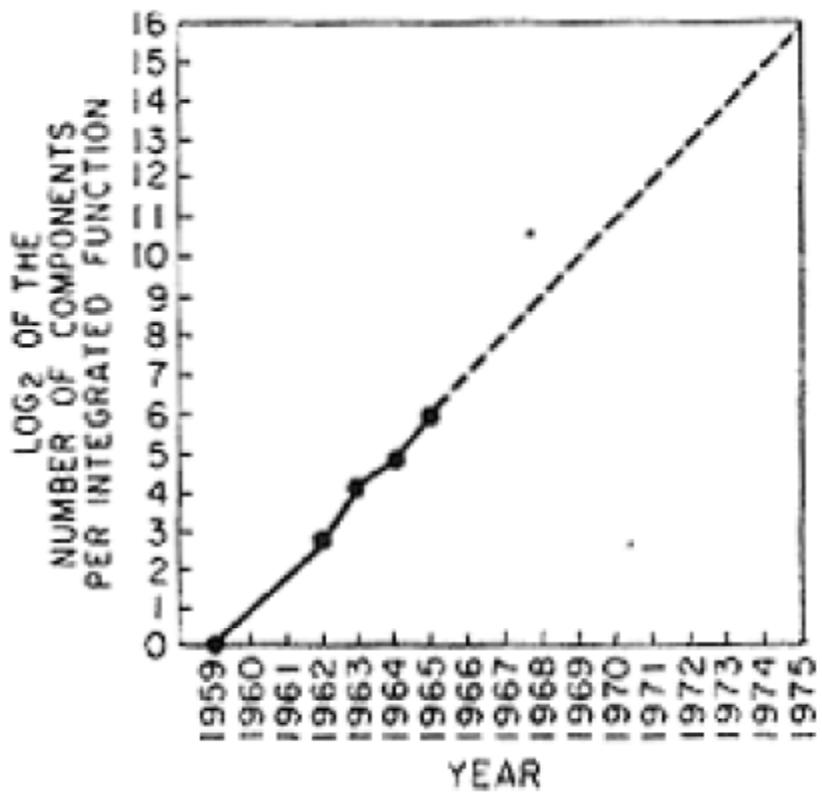
# Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squaring many as 65,000 components on a single silicon chip.

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor Division of Fairchild Camera and Instrument Corp.

Electronics, Volume 38, Number 8, April 19, 1965



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The experts look ahead

# Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

Objective: reduce the cost per single transistor



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# Birth of the PIC Concept

*"There is a conviction that the new miniaturized optical circuitry will prove useful... We must wait a while longer to find out how useful this new technology will become."*



## THE BELL SYSTEM TECHNICAL JOURNAL

DEVOTED TO THE SCIENTIFIC AND ENGINEERING  
ASPECTS OF ELECTRICAL COMMUNICATION

Volume 48

September 1969

Number 7

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### Integrated Optics: An Introduction

By STEWART E. MILLER

(Manuscript received January 29, 1969)

*This paper outlines a proposal for a miniature form of laser beam circuitry. Index of refraction changes of the order of  $10^{-2}$  or  $10^{-3}$  in a substrate such as glass allow guided laser beams of width near 10 microns. Photolithographic techniques may permit simultaneous construction of complex circuit patterns. This paper also indicates possible miniature forms for a laser, modulator, and hybrids. If realized, this new art would facilitate isolating the laser circuit assembly from thermal, mechanical, and acoustic ambient changes through small overall size; economy should ultimately result.*

#### I. INTRODUCTION

Laboratory work and experimental repeater work at laser wavelengths (0.4 to 10  $\mu\text{m}$ ) has been carried out by interconnecting the oscillators, modulators, detectors, and so on, using a form of extremely short-range radio. A freely propagating beam has been reflected around corners, occasionally refocused with lenses to avoid energy loss resulting from beam spreading, and often sheltered by tubular enclosures from refractive distortions resulting from thermal gradients in the ambient air. Typical separations between components range from a few centimeters to a foot; aggregations of apparatus in a single-channel experimental laser repeater are measured

2059



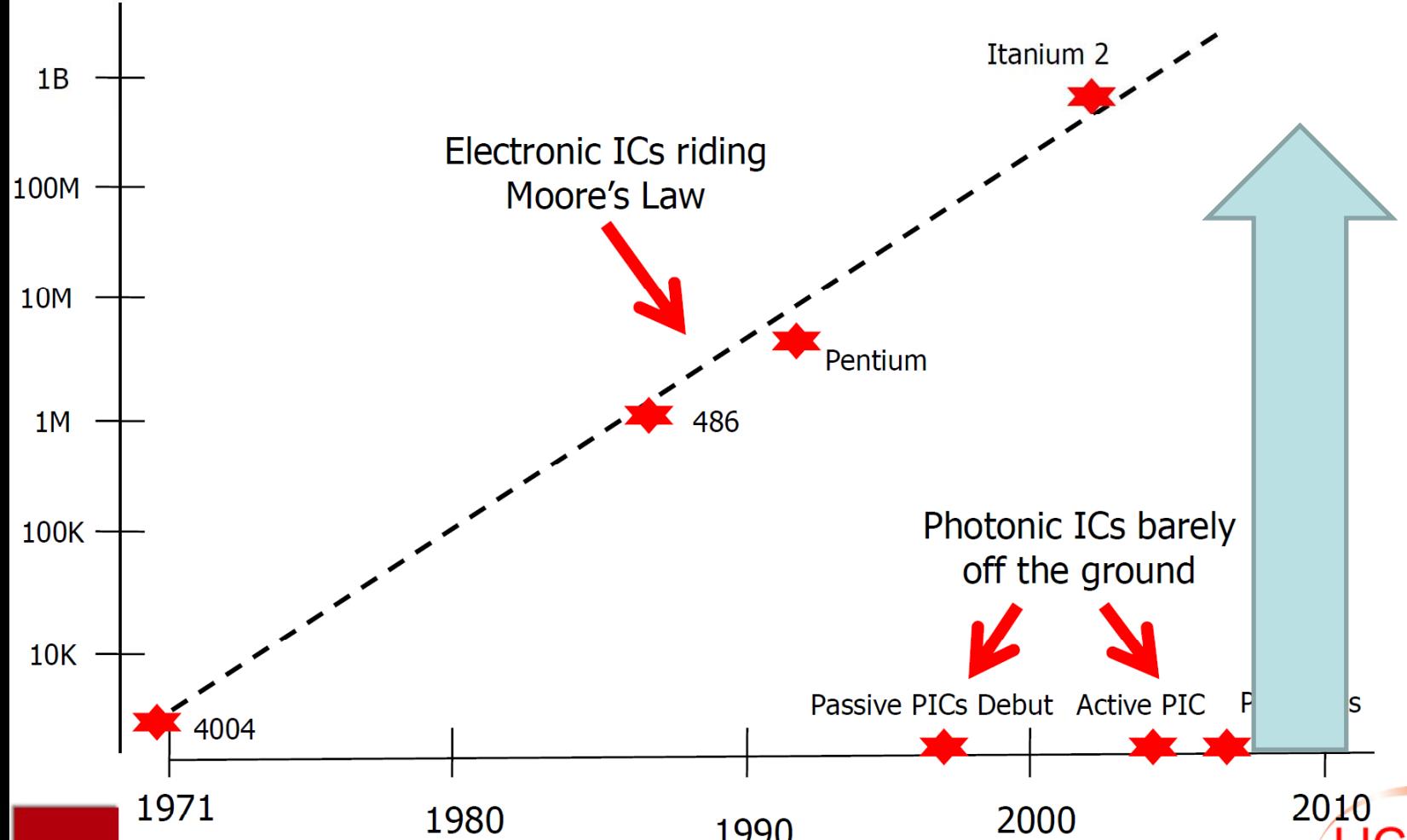
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29 January 1969

# Comparing Technology Progress

Functions per Chip



## Technology Comparison: Optics vs. ICs

| Technologies                   | Semiconductor IC | Optical Components                                      |
|--------------------------------|------------------|---|
| Repeatable building block      | Transistors      | <b>None</b><br>(LD, PD, Mod, Filter, Isolator...)       |
| Uniform material base          | Silicon          | <b>None</b><br>(InP, GaAs, Si...)                       |
| Dominant manufacturing process | CMOS             | <b>None</b><br>(Hybrid, monolithic, active, passive...) |

Source: J. P. Morgan

No standardized technology for optical components manufacturing

## Technology Comparison: Optics vs. ICs vs. Silicon Photonics

| Technologies                   | Optical Components                               | Semiconductor IC | Silicon Photonics       |
|--------------------------------|--|------------------|-------------------------|
| Repeatable building block      | None<br>(LD, PD, Mod, Filter, Isolator...)       | Transistors      | LD,PD, microrings, .... |
| Uniform material base          | None<br>(InP, GaAs, Si...)                       | Silicon          | Silicon                 |
| Dominant manufacturing process | None<br>(Hybrid, monolithic, active, passive...) | CMOS             | CMOS                    |

Source: J. P. Morgan

No standardized technology for optical components manufacturing

# Silicon photonics

Photonic devices produced within  
standard silicon factory and with  
standard silicon processing



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# Silicon pro's and cons

- Transparent on 1.3-1.5  $\mu\text{m}$
  - CMOS compatibility
  - Low cost
  - High index contrast, small footprint
- 

- No electro-optic effect
- No detection in 1.3-1.5  $\mu\text{m}$  region
- High index contrast coupling
- Lacks efficient light emission



# The Opportunity of Silicon Photonics

- Enormous (\$ billions) CMOS infrastructure, process learning, and capacity
  - Draft continued investment in Moore's law
- Potential to integrate multiple optical devices
- Micromachining could provide smart packaging
- Potential to converge computing & communications



To benefit from this optical wafers  
must run alongside existing product.  
**CMOS PHOTONICS**



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# Cost = paradigm change

- 200 mm Si wafer has 125,000 - 0.5 mm sized dies
- Cost processed CMOS wafers \$2,000,000
- Cost per die: \$16
- Laser size: 10x100 microns.
- Cost per laser: \$ 0.064
- This is just like estimating the cost of transistors. They are free. Only the PIC cost matters.
- Emphasis is moved from components to the system



# Silicon photonics

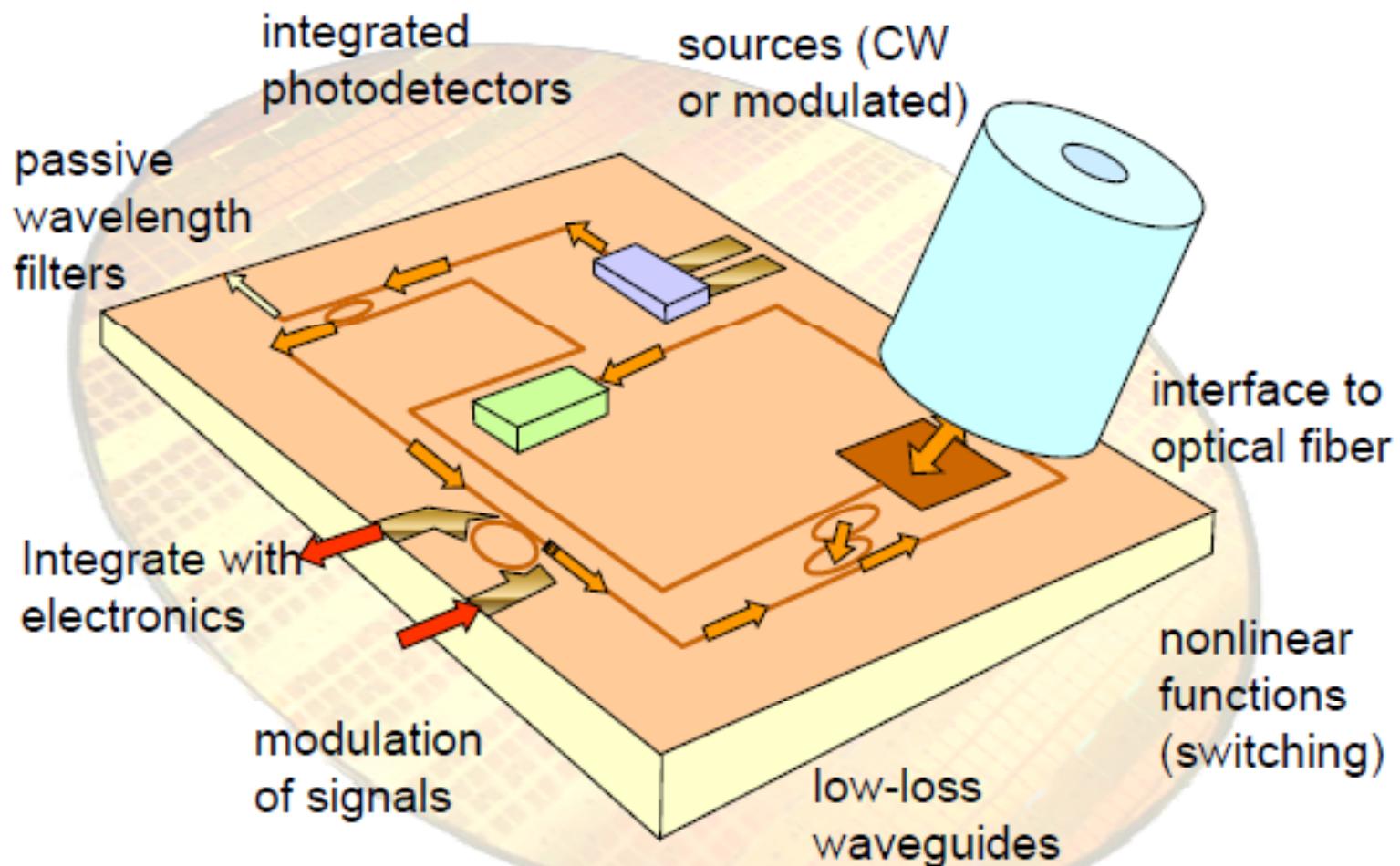
## Basic building blocks



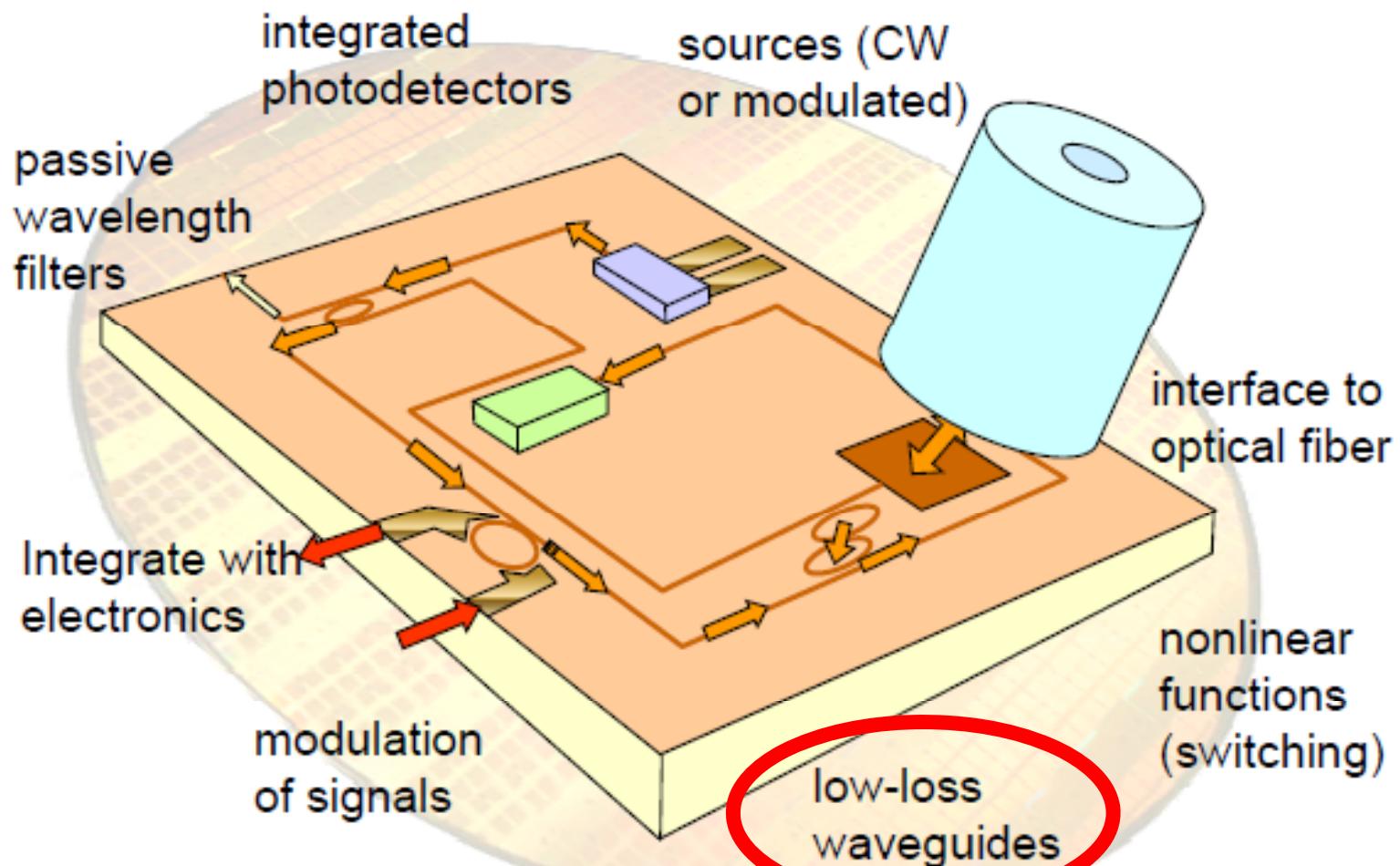
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# Functions to be integrated



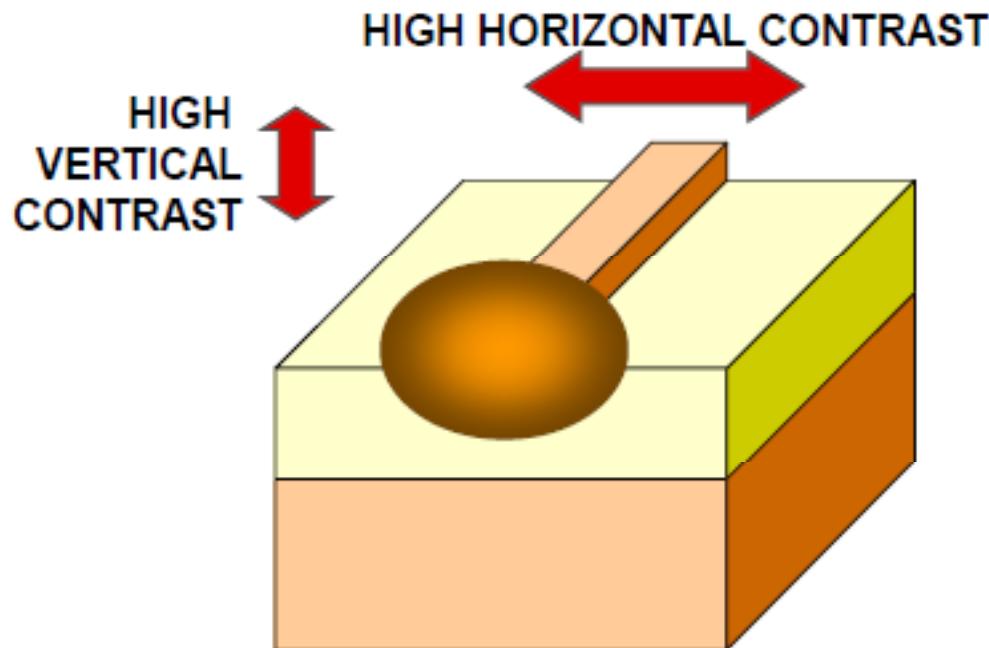
# Functions to be integrated



# SOI Photonic Wires

## High-contrast waveguide

- Large index contrast: 3.45 to 1.45
- Submicron cross section:  $450 \times 220\text{nm}^2$
- Sharp bends ( $R \sim 2-3\mu\text{m}$ )



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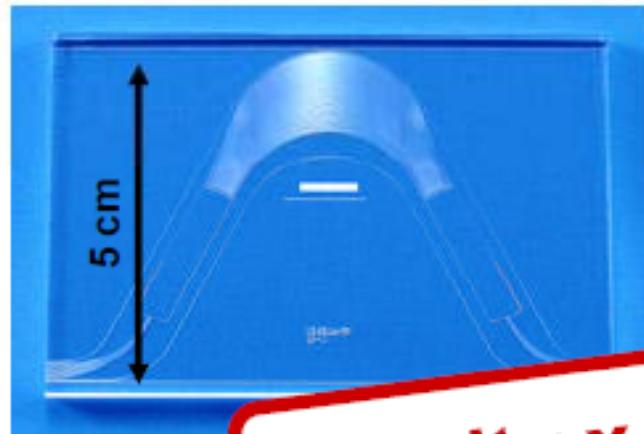
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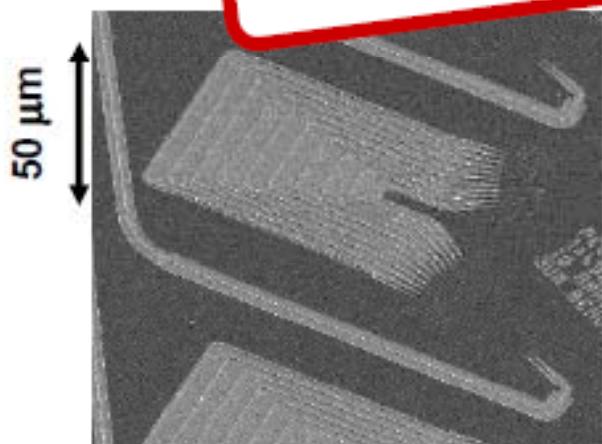
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# Larger-scale integration

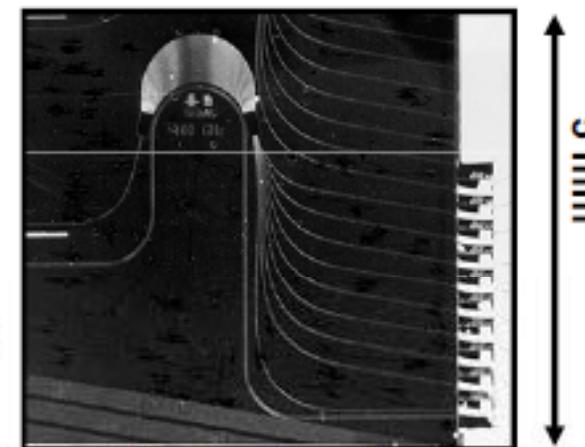


Low Contrast - Fiber Matched  
(silica or polymer based)  
Bend Radius ~ 5 mm  
Size ~ several cm<sup>2</sup>



Density × 10<sup>6</sup>

Ultra-high Contrast  
(Silicon on Insulator)  
Bend Radius < 5 μm



Medium Contrast  
(InP-InGaAsP)  
Bend Radius ~ 500 μm

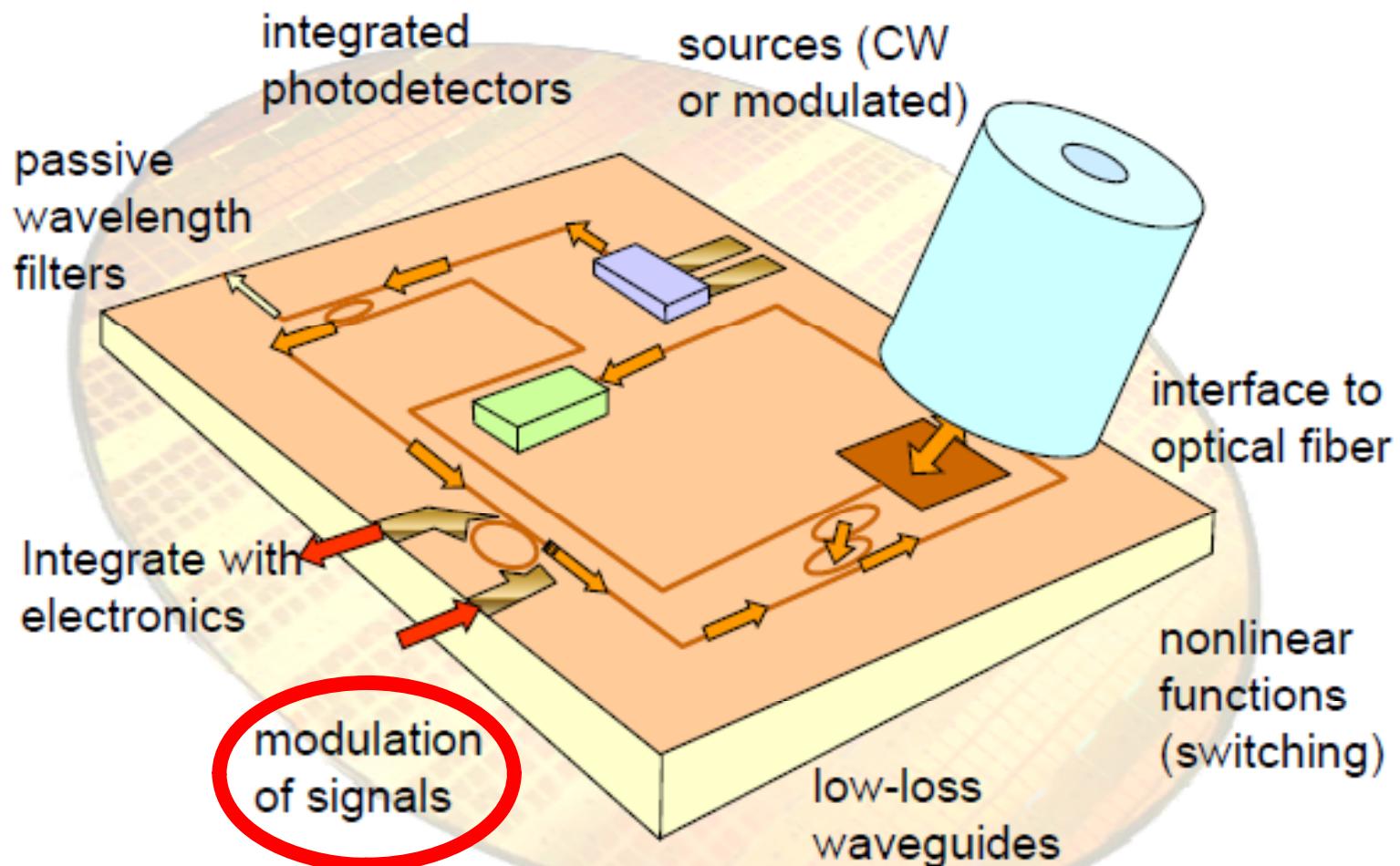


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# Functions to be integrated



# Modulator

- Because of its crystal structure, silicon is not a useful conventional electro-optic material
- Because of its indirect bandgap, silicon has no near bandgap nonlinearities
- Thermo-optical effect is strong but slow

The only effect that is left is the free carrier or Drude effect

$$\Delta n = - \left[ 8.8 \times 10^{-22} \Delta N + 8.5 \times 10^{-18} (\Delta P)^{0.8} \right]$$

$$\Delta \alpha = \left[ 8.5 \times 10^{-18} \Delta N + 6.0 \times 10^{-18} (\Delta P) \right]$$

*R.A. Soref and B.R. Bennett, IEEE JQE 23, 123 (1987)*



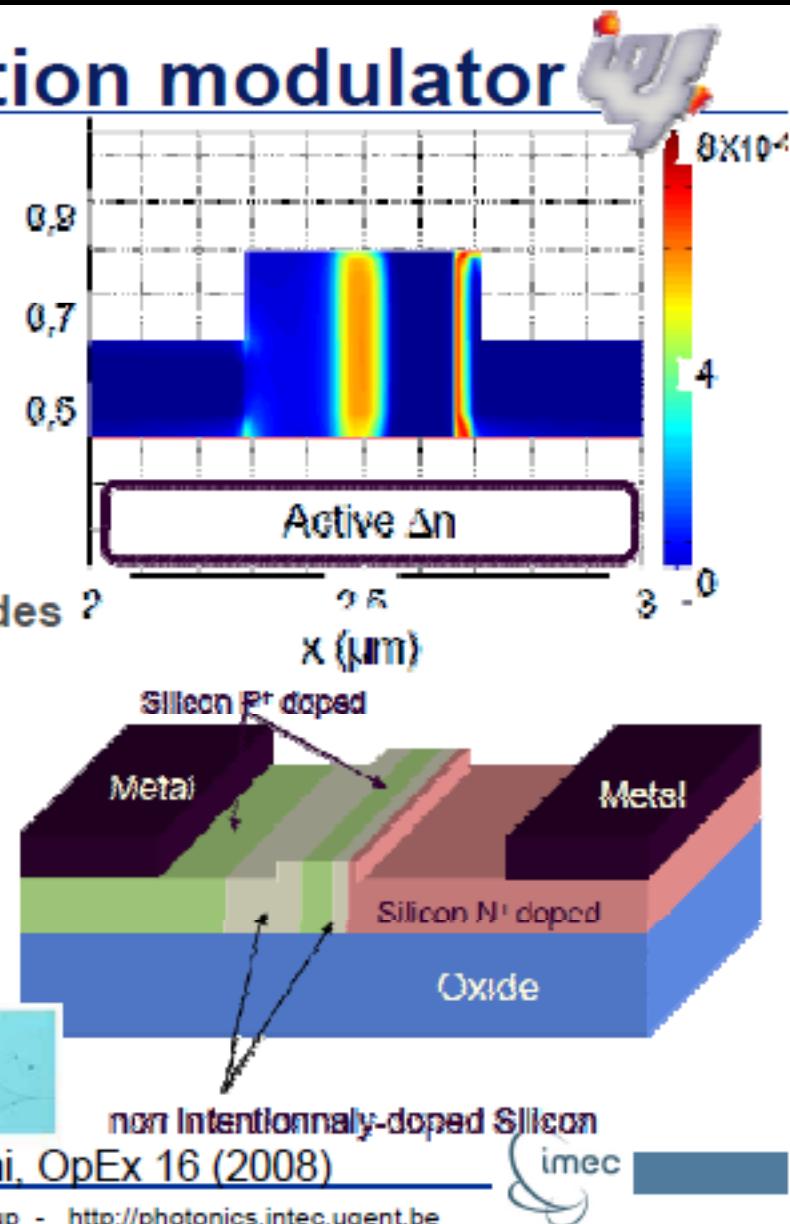
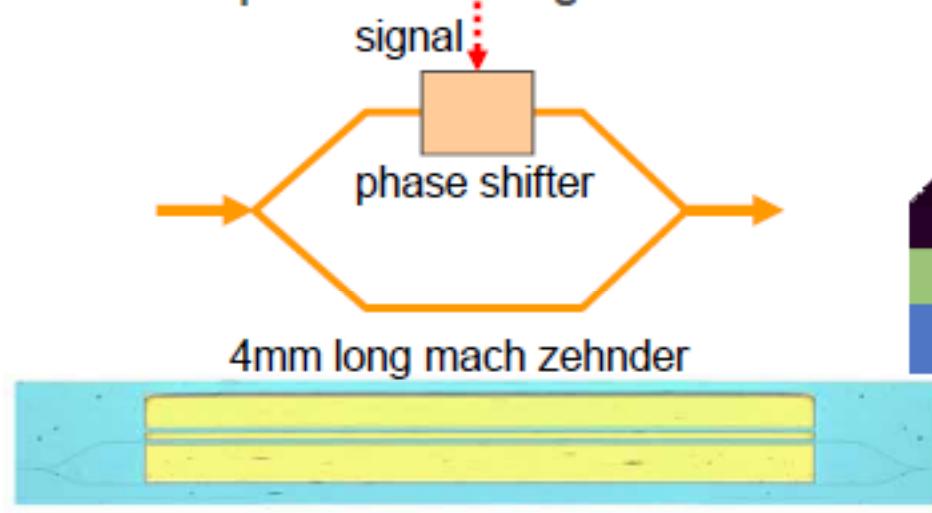
# Example: depletion modulator

## Complex multi-doping profile

- Larger index change
- Lower RC

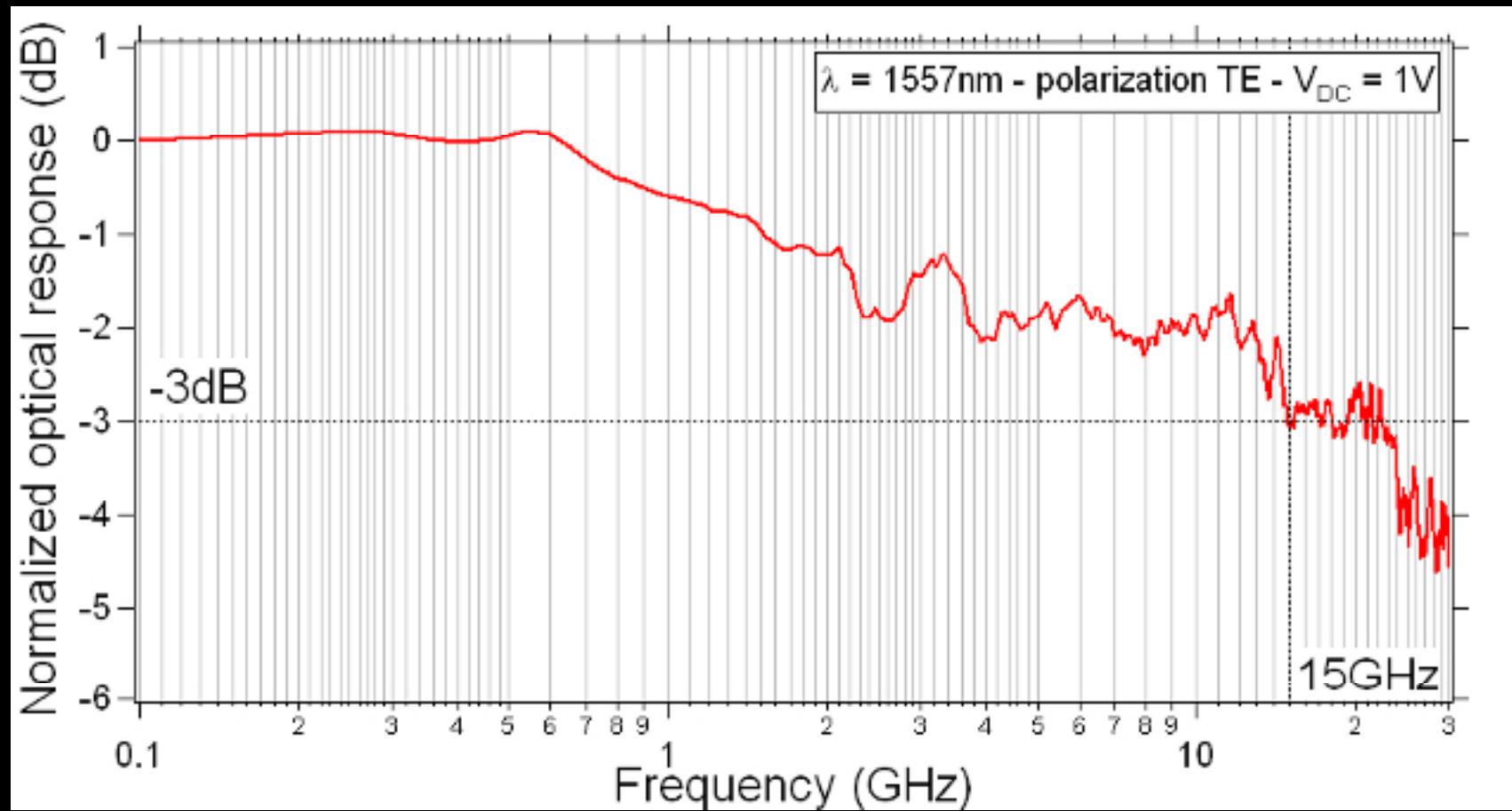
But

- Still a long device (4mm)
- Requires travelling wave electrodes

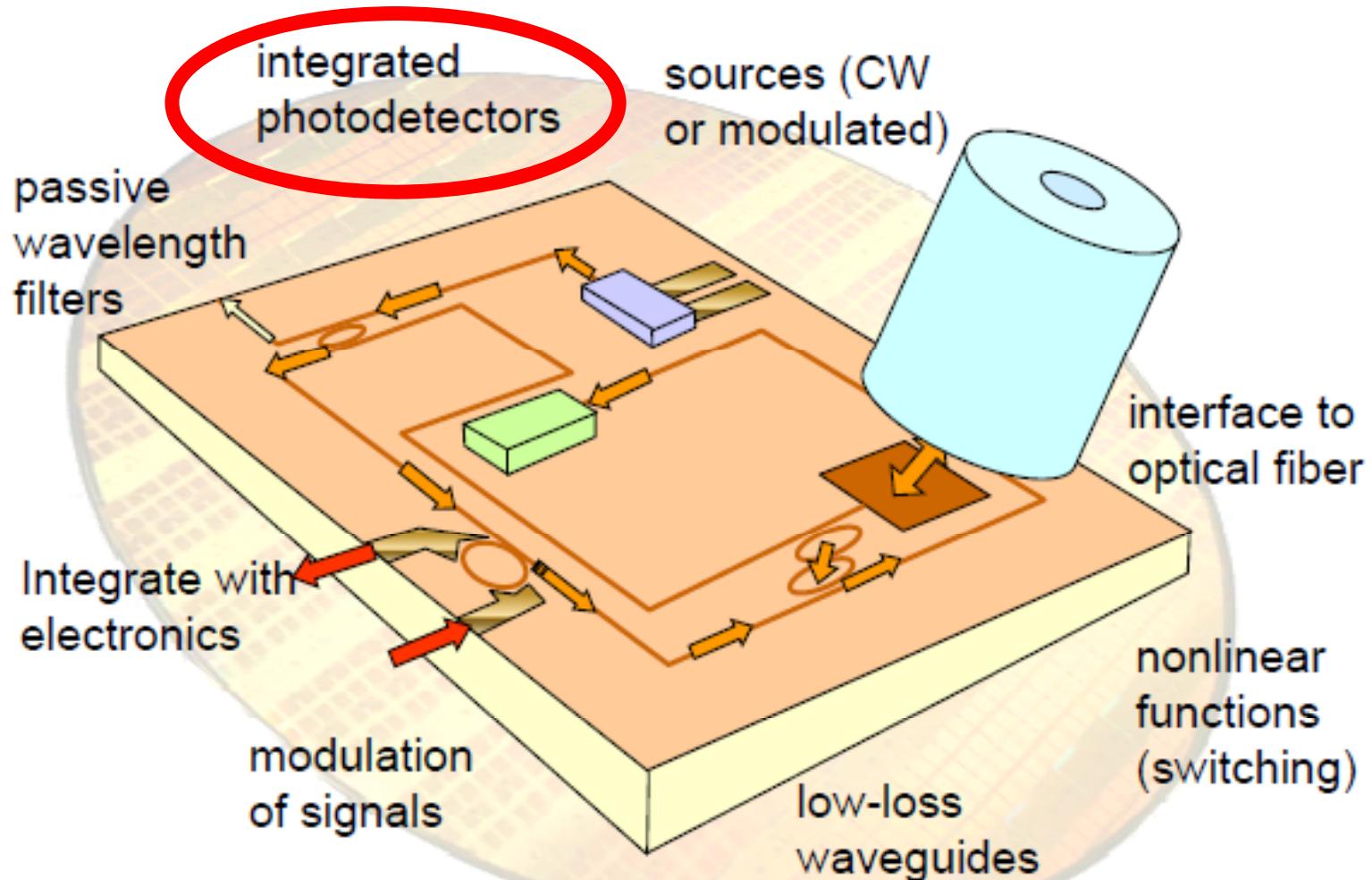


D. Marris-Morini, OpEx 16 (2008)

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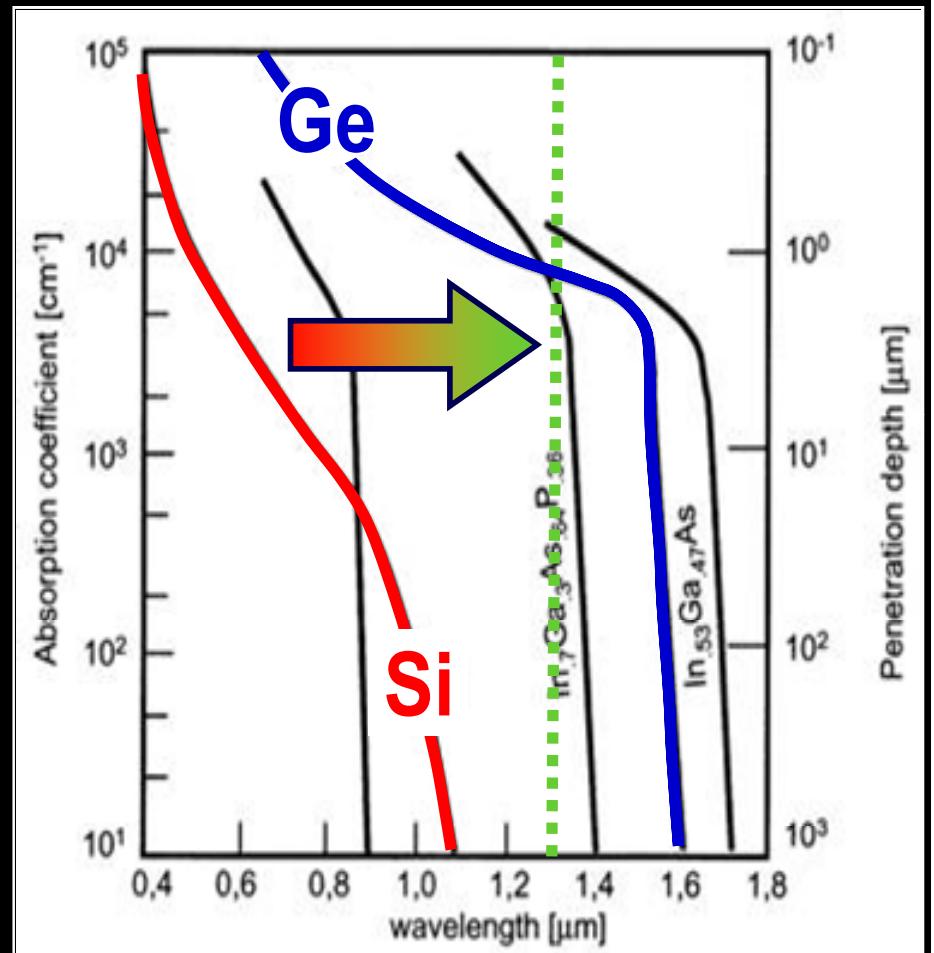


# Functions to be integrated

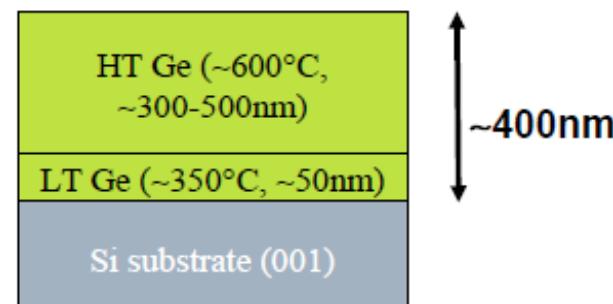


# Photodetection

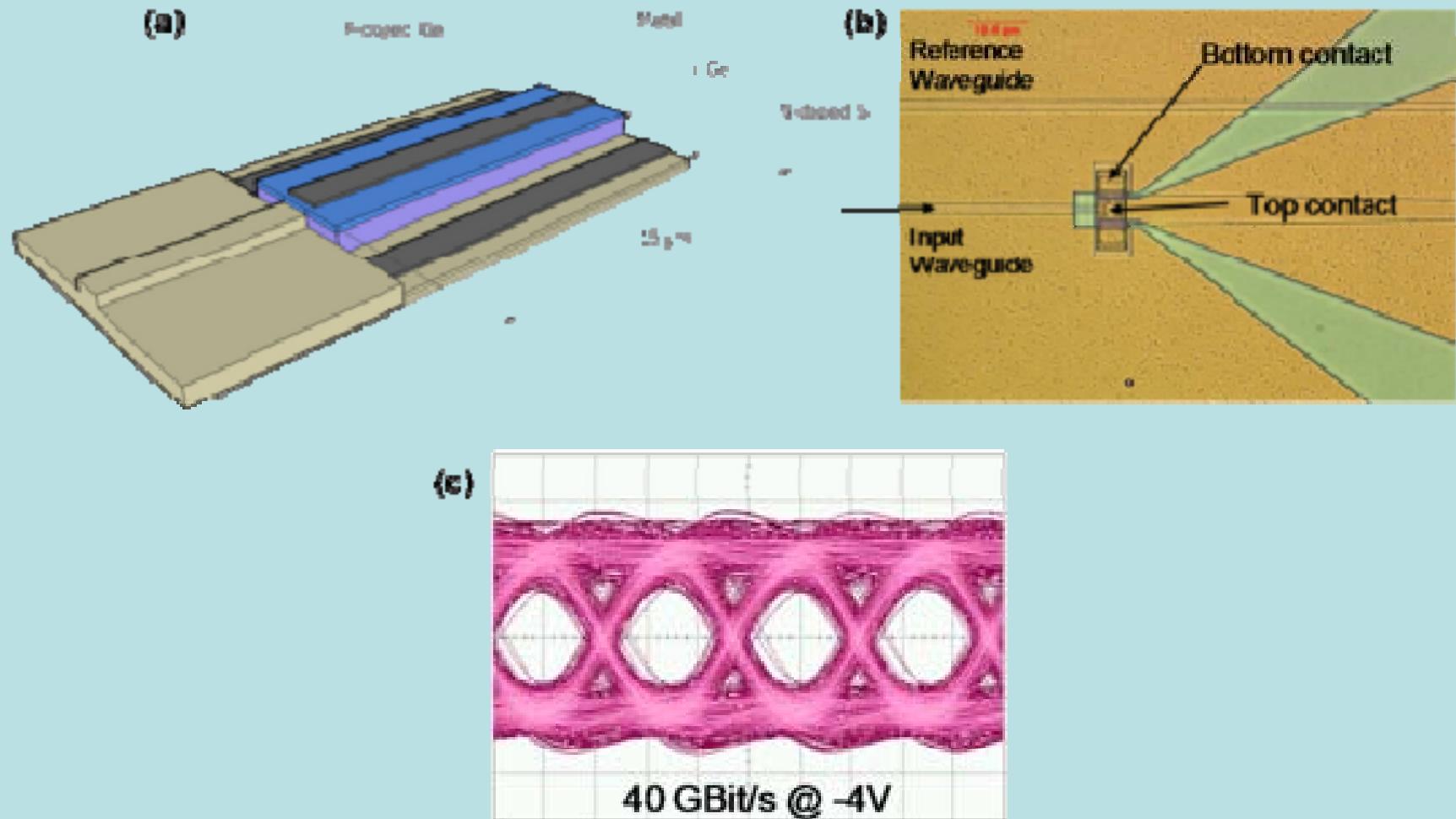
- **Silicon does not absorb IR well**
  - Use hybrid approach
  - Use SiGe or strained Ge
  - Use damaged silicon



- Two-step growth process:
  - Direct growth of Ge on Si using a low temperature (~350°) CVD process  
⇒ thin (a few 10nm) highly-dislocated Ge layer
  - Growth of a thick Ge layer (a few 100nm) at a higher temperature (~600°)  
⇒ high quality Ge absorbing layer
- Thermal annealing to reduce the dislocation density

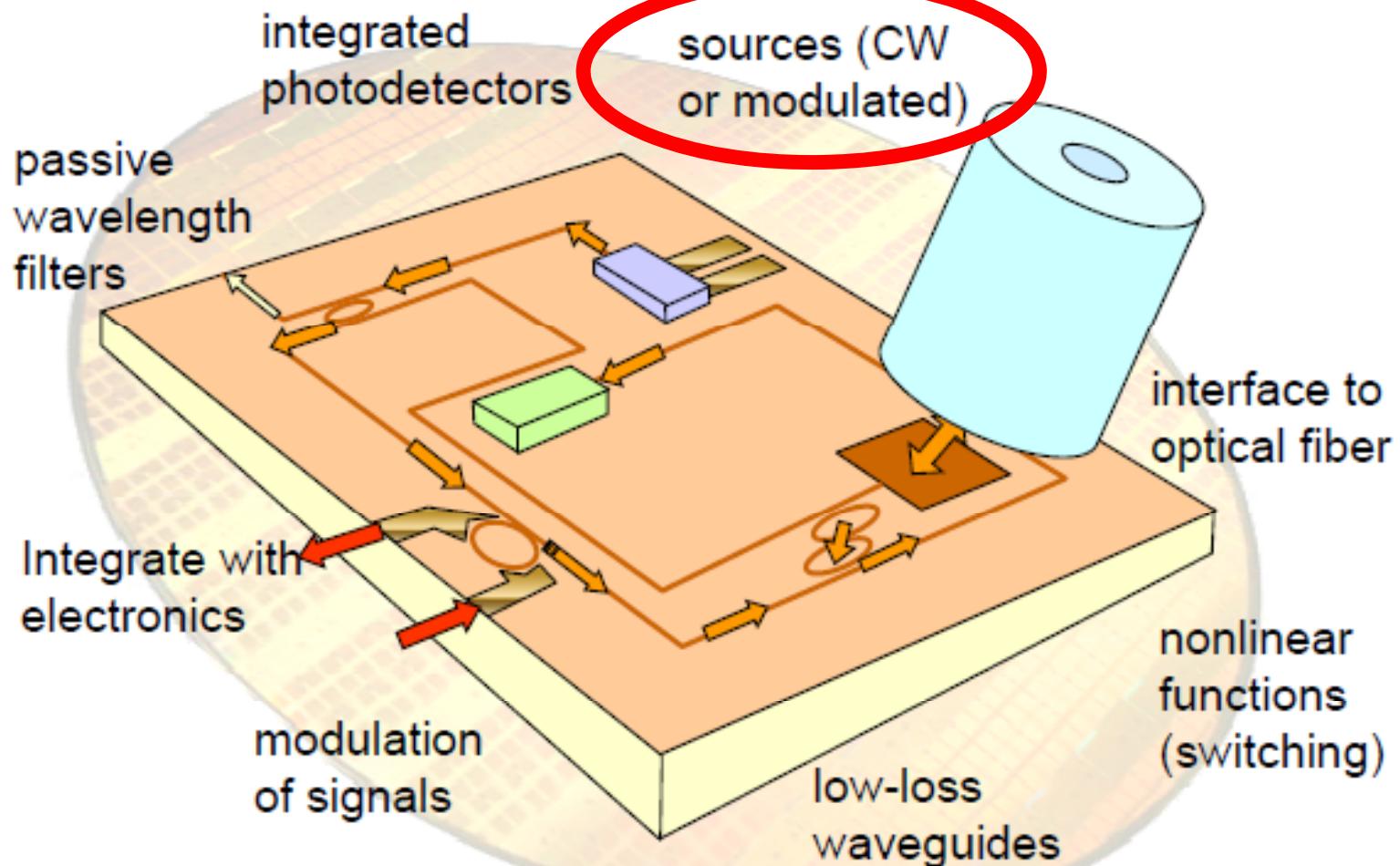


# Ge photodector



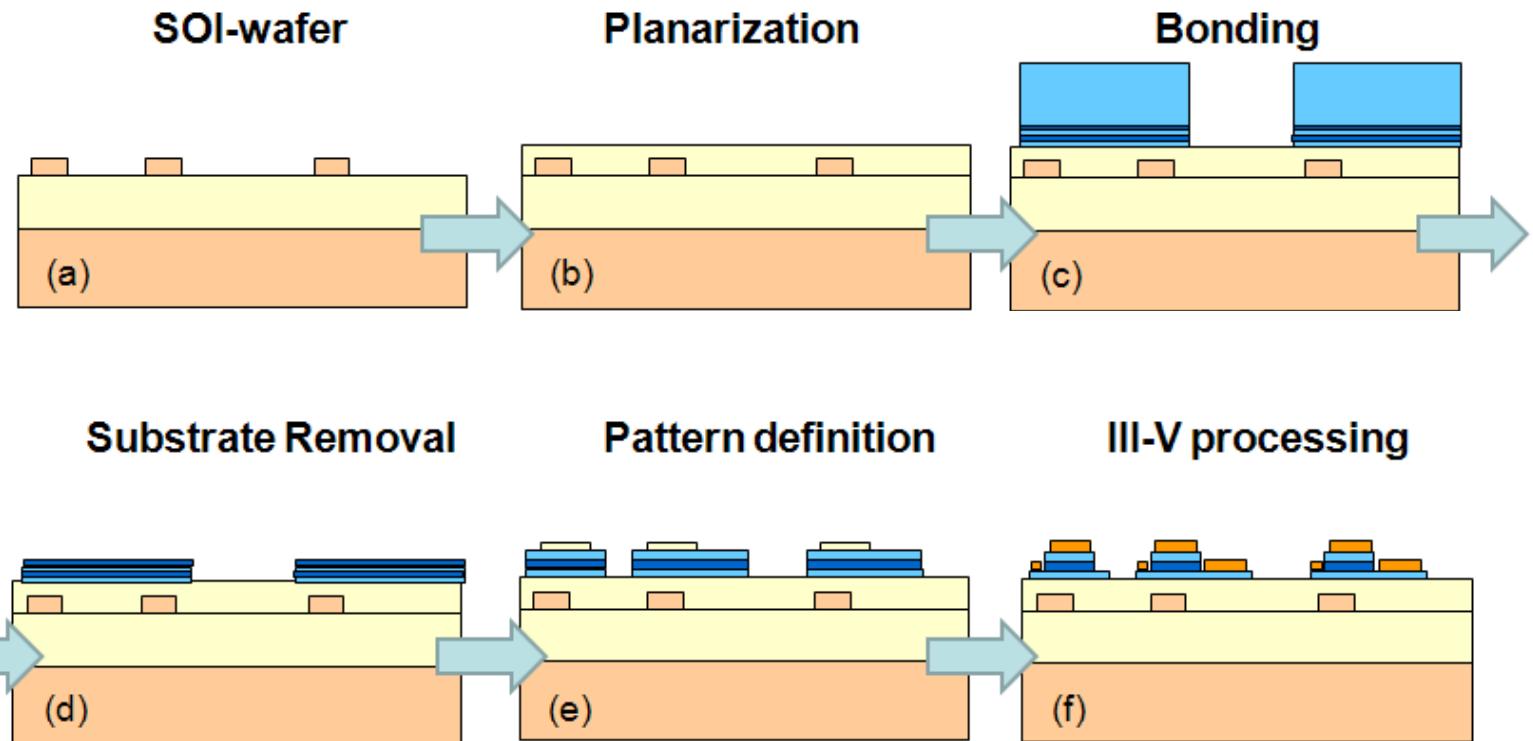
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# Functions to be integrated

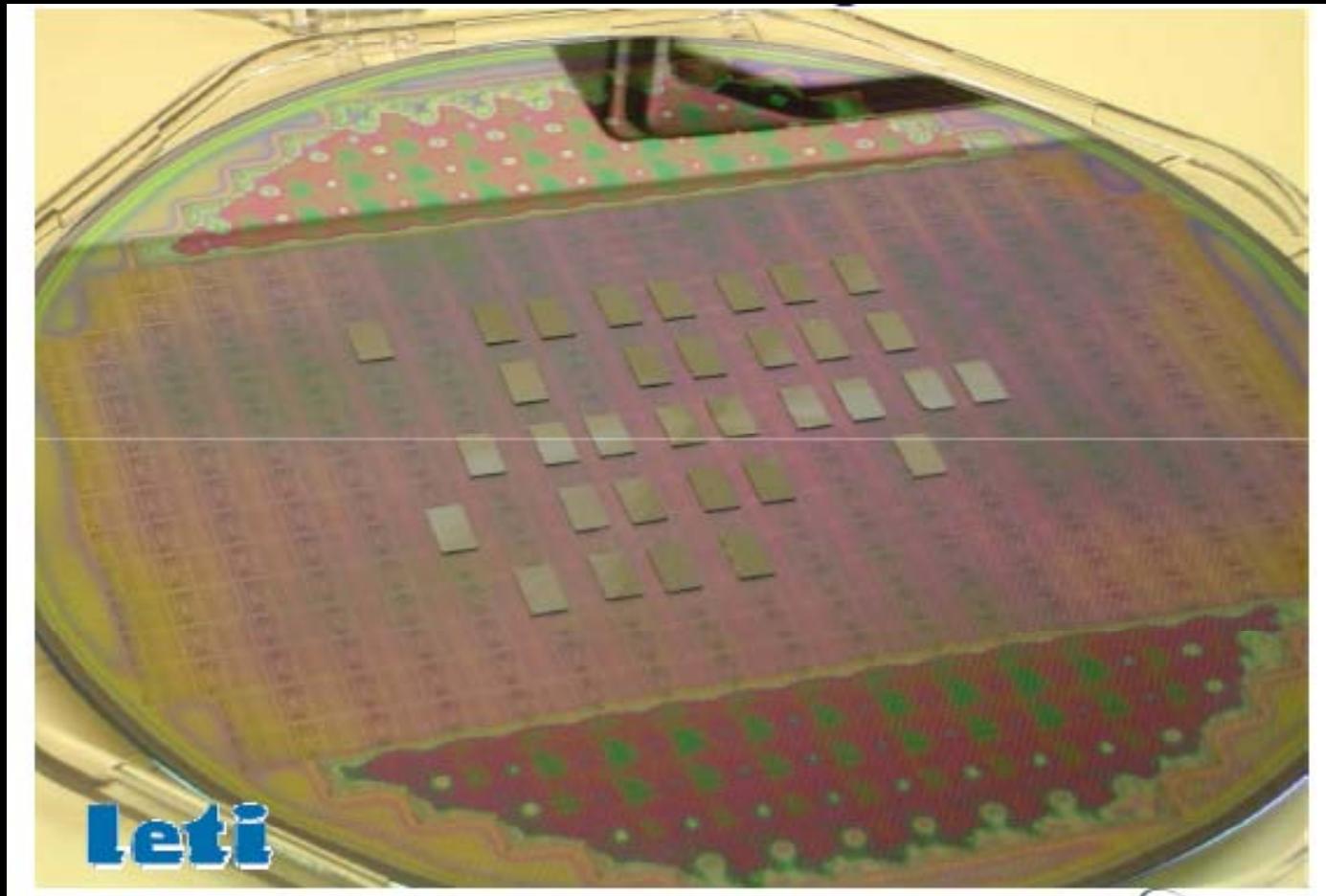


# III-V heterogeneous integration for the laser source

## Integration Scheme



# III-V heterointegration for the laser source



**leti**

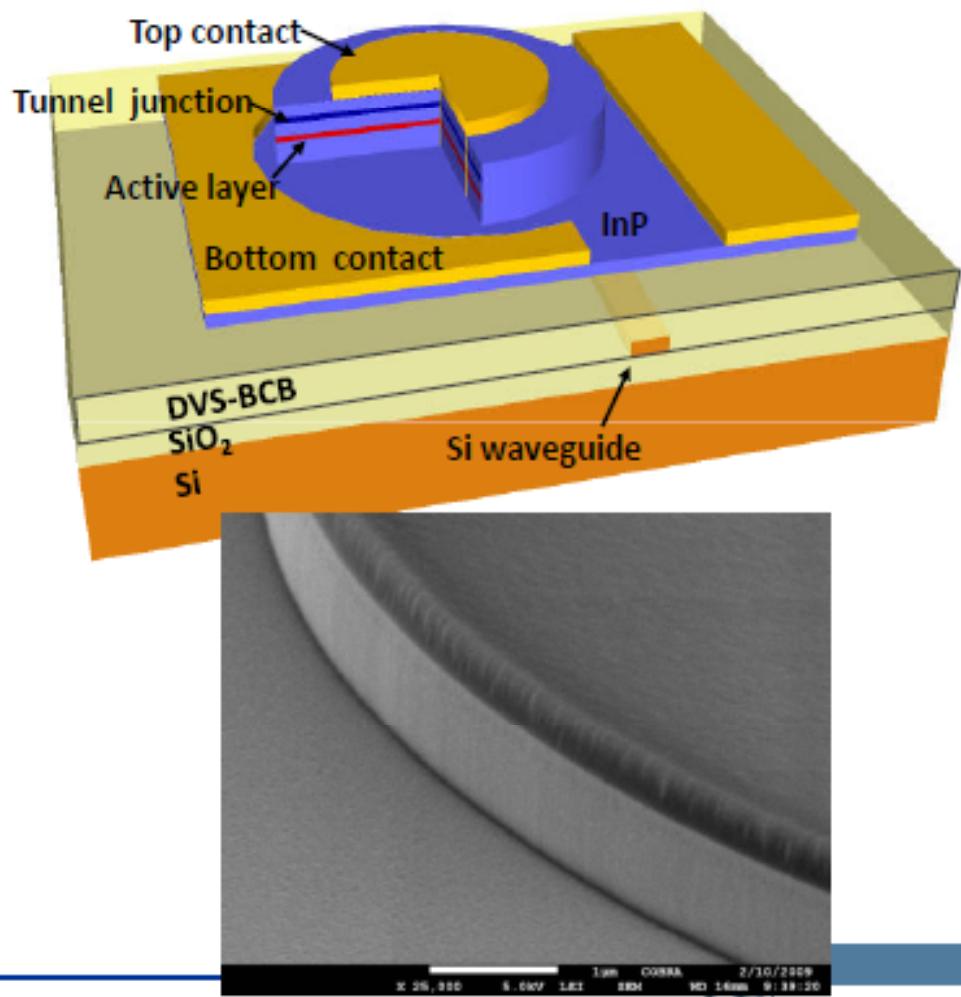


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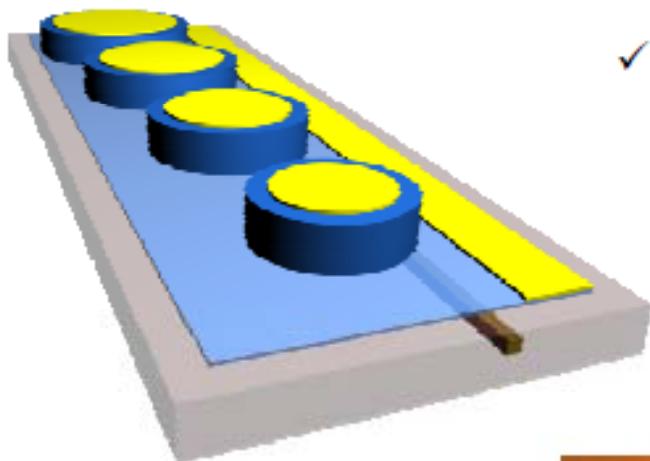


# InP microdisk laser

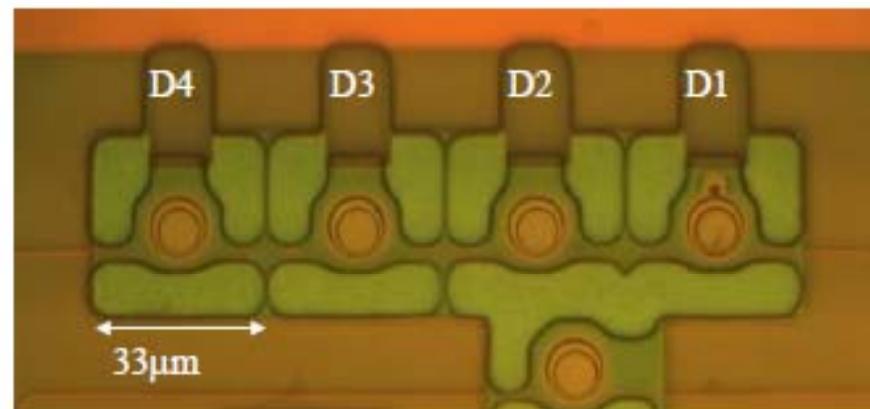
- 7.5 um diameter
- 600 nm height
- Adhesive bonding  
(BCB ~ 250 nm)
- Evanescent coupling  
to Si Waveguide



# Multi-wavelength Laser



- ✓ Several (4) microdisks with different diameters are cascaded on one bus SOI waveguide.



J. Van Campenhout, L. Liu, et al, PTL 20, 1345, (2008).

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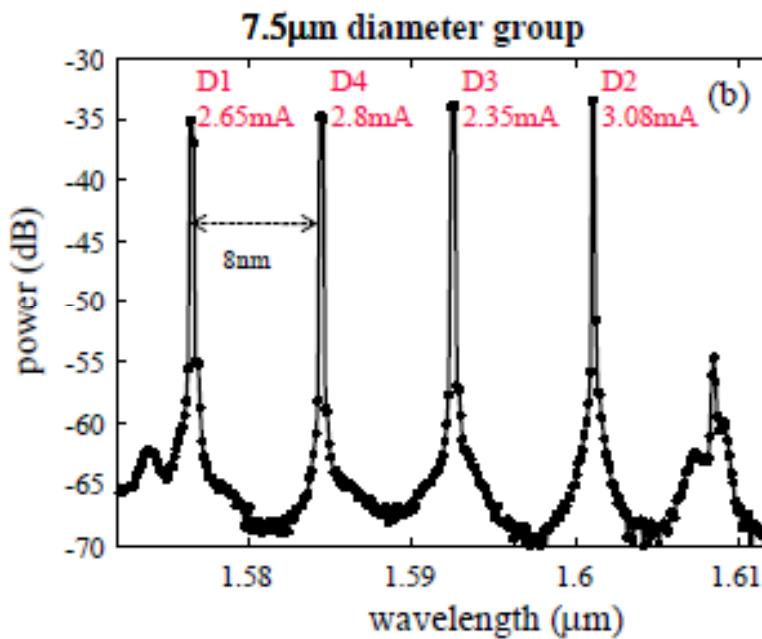
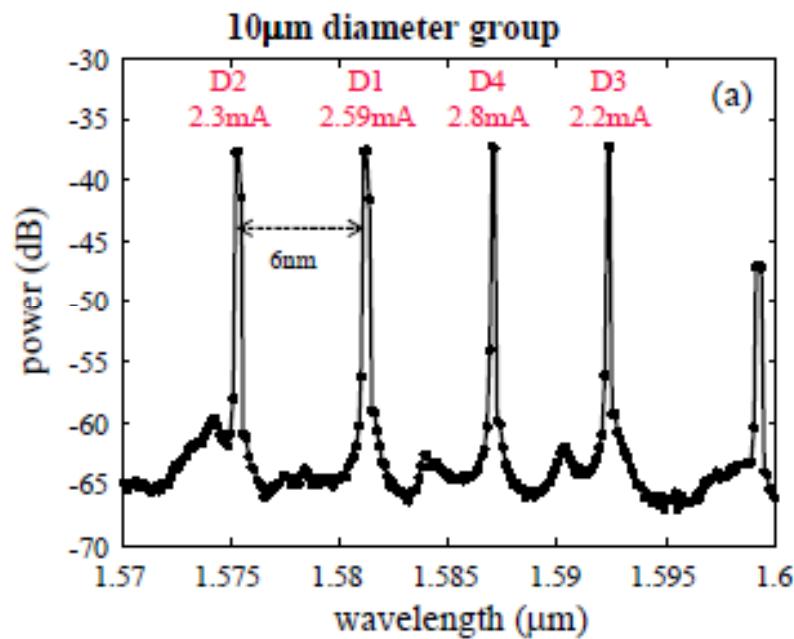
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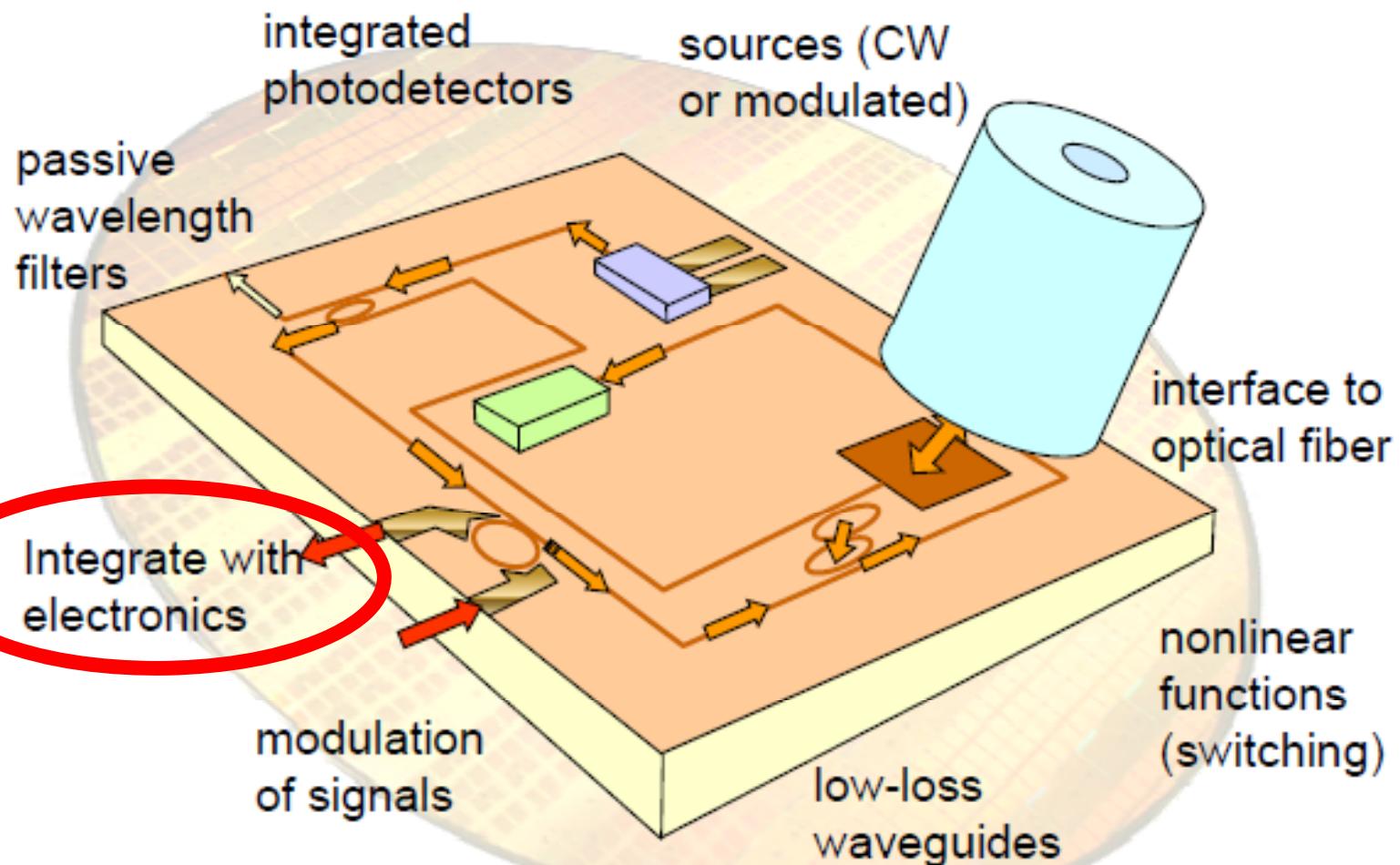
# Multi-wavelength Laser



- Uniform peak power was obtained by adjusting the driving current of each individual disk laser.



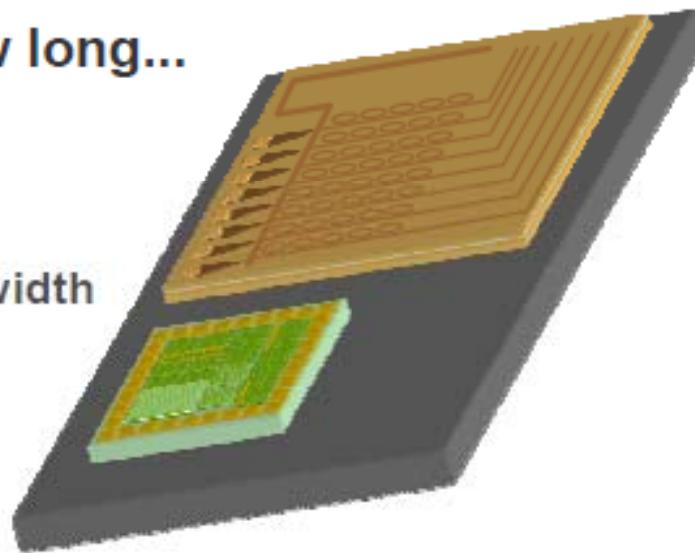
# Functions to be integrated



# Co-packaging?

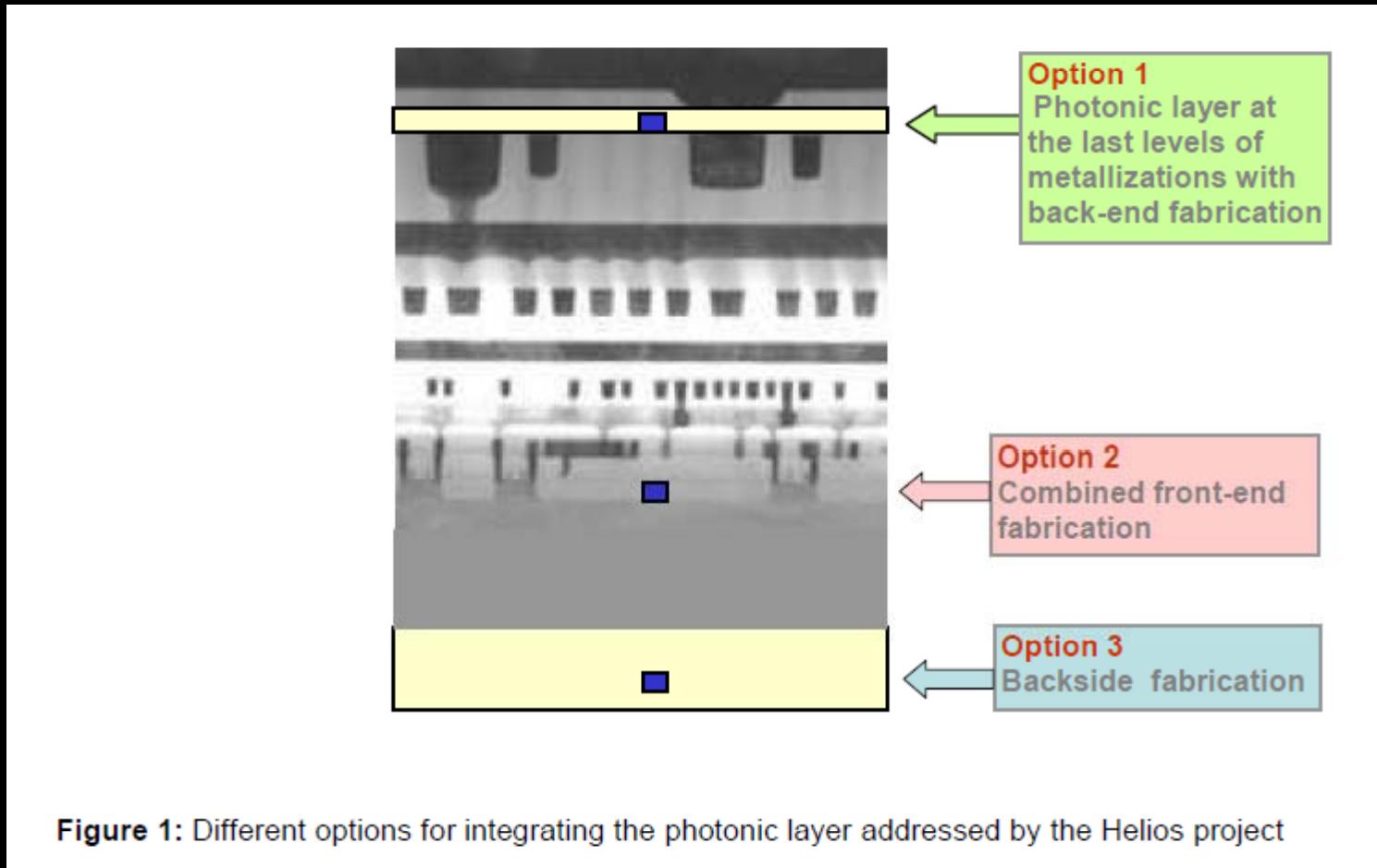
Works for now, but for how long...

- limited integration density
  - edge vs. area
- long distance = lower bandwidth



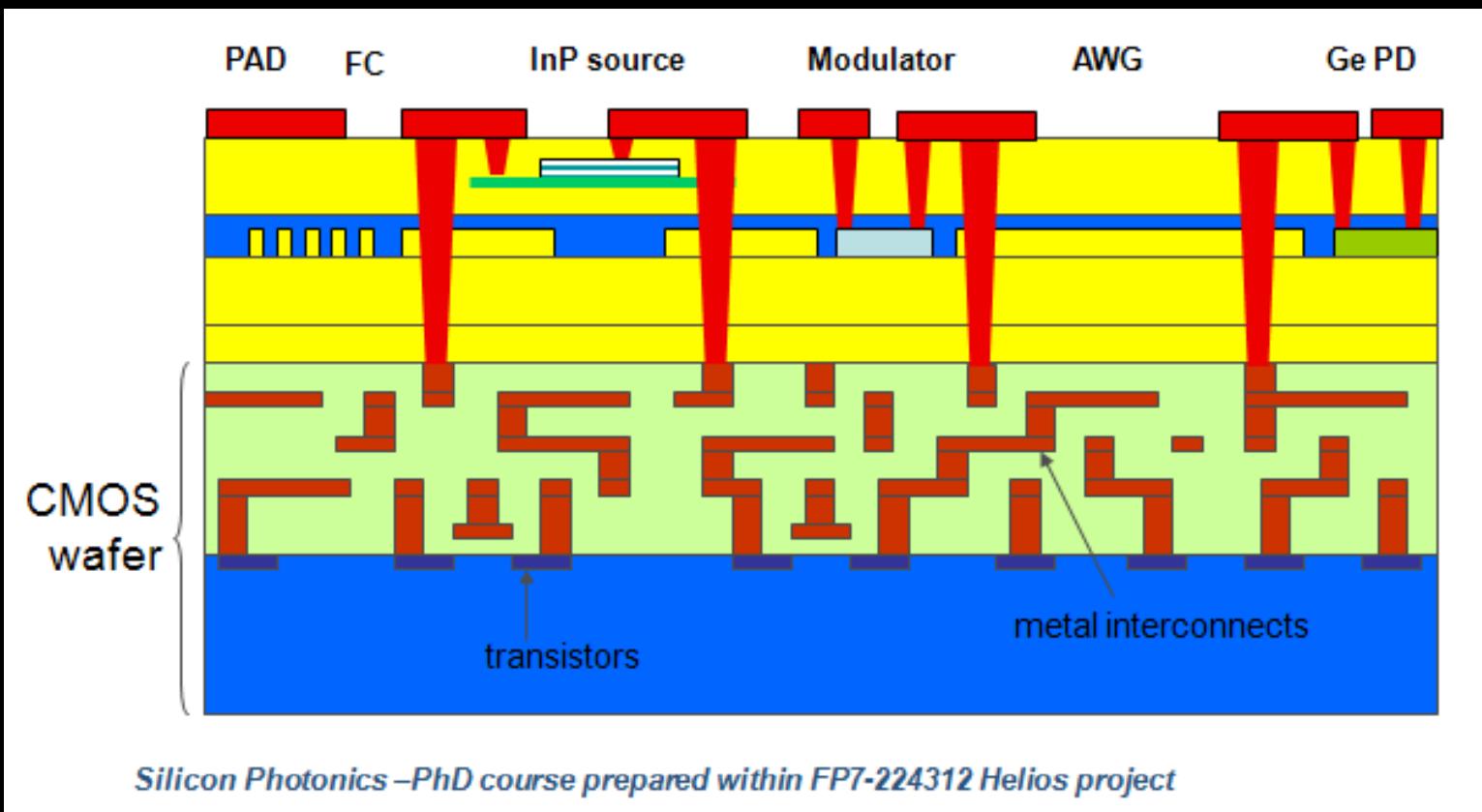
Integrate photonics with CMOS  
in a more scalable way

# Where should we integrate the photonics layer ?



**Figure 1:** Different options for integrating the photonic layer addressed by the Helios project

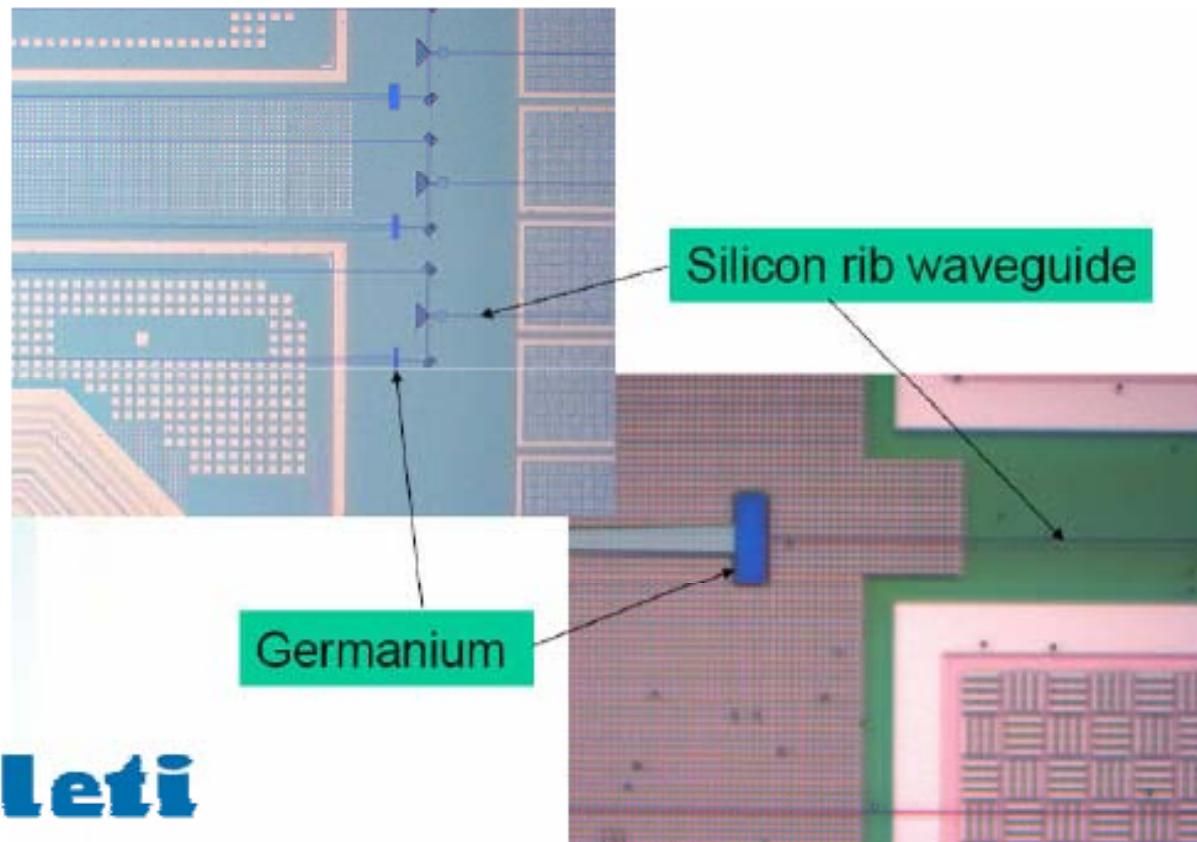
# Options 1



# Options 1

## CMOS + Photonics wafer bonding

Photonics wafer on top of CMOS wafer



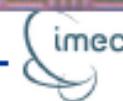
**leti**

J.M. Fedeli et al. Proc. SPIE 6125 (2006)



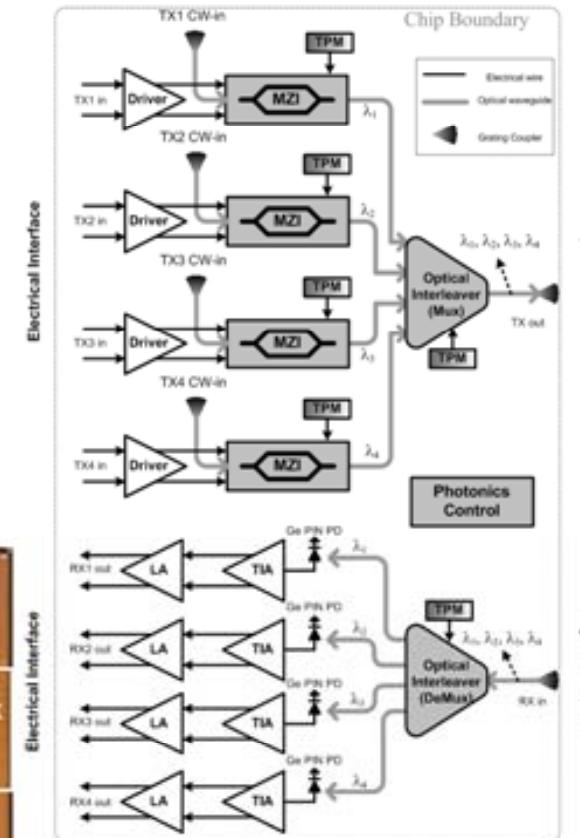
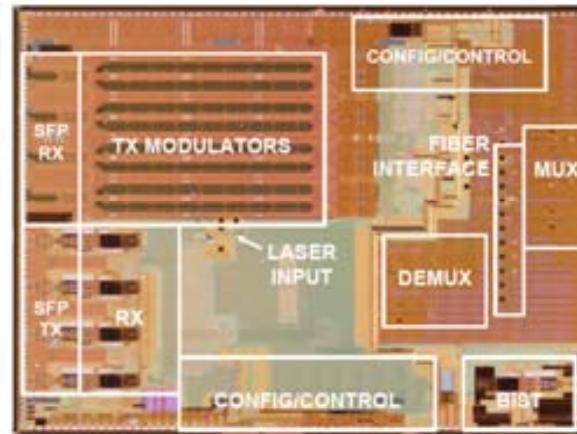
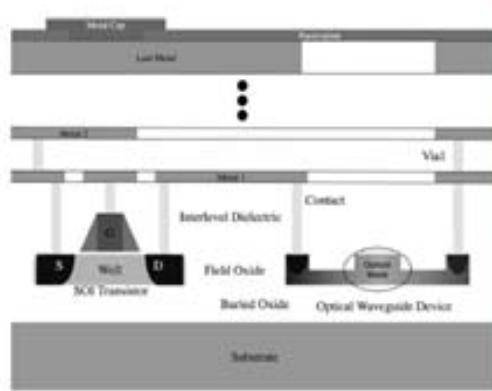
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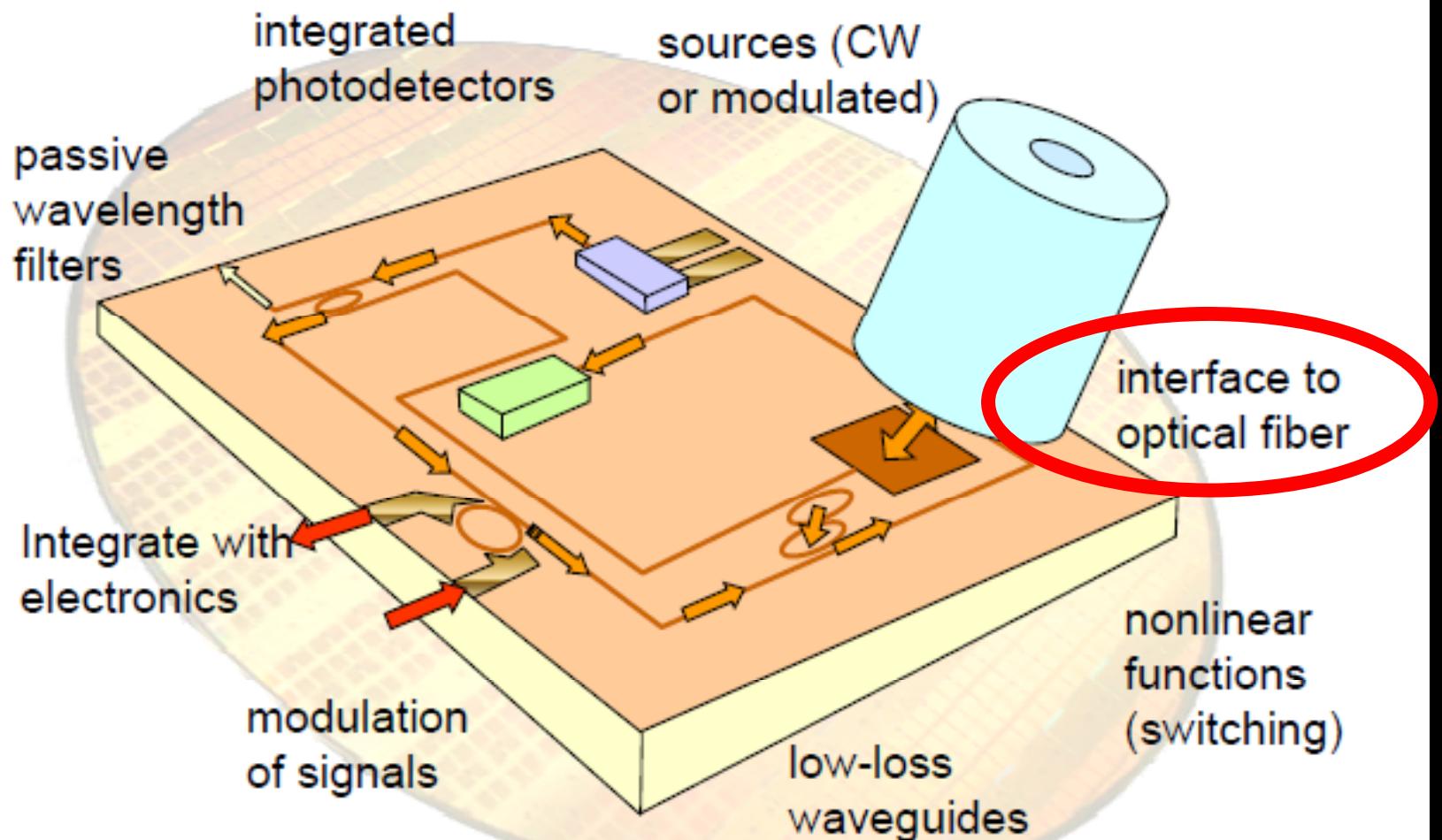


## Option 2: Luxtera approach

- Proprietary SOI CMOS 130nm technology
- Proprietary library for IC design
- Flip chip bonded lasers or external WDM lasers
- Surface gratings fiber couplers
- MUX and DEMUX with controlled MMI
- 10Gb/s modulator based on lateral Si depletion
- 20GHz Ge photodetectors
- Electronic control of optical devices



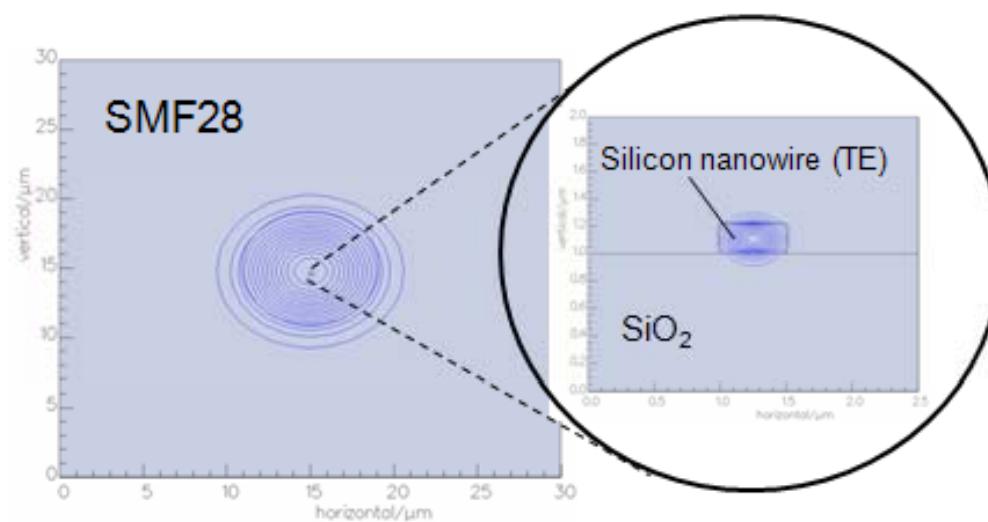
# Functions to be integrated





## Major obstacle in silicon photonics

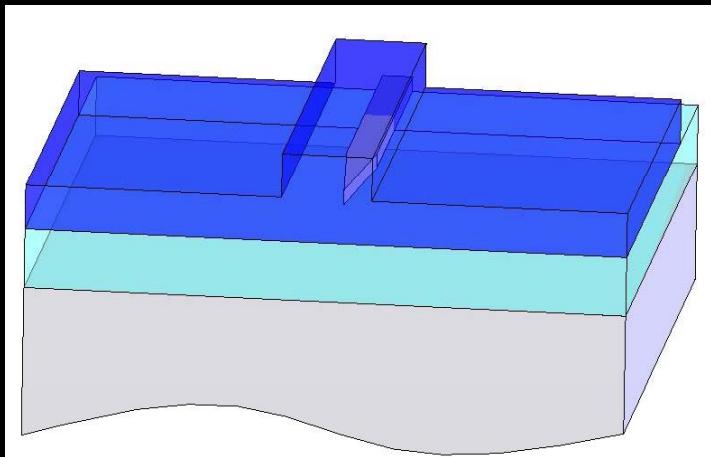
MFD of fiber and waveguides do not match



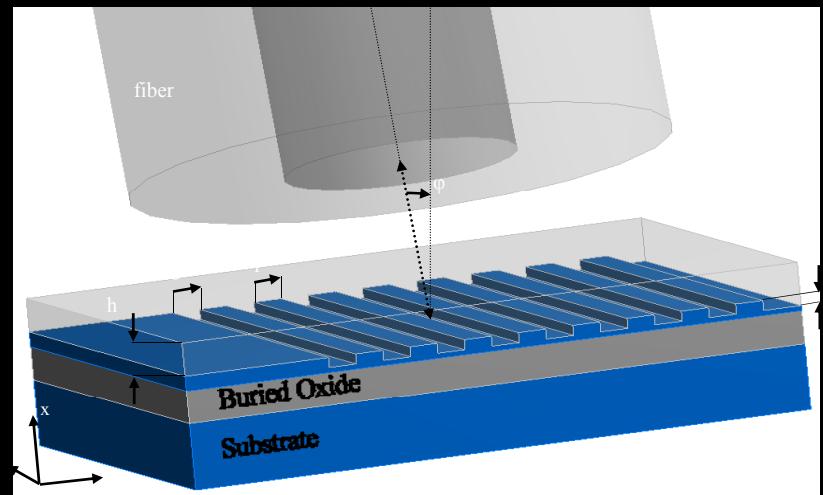
# This requires

Spotsize conversion structures

*Lateral coupling*



*Vertical coupling*



- typically based on inverted tapers
- spotsize:  $\sim 3 \mu\text{m}$

- typically based on gratings
- spotsize:  $\sim 10 \mu\text{m}$



## Example - g-Pack



Fraunhofer Institut  
Zuverlässigkeit und  
Mikointegration



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# Outline

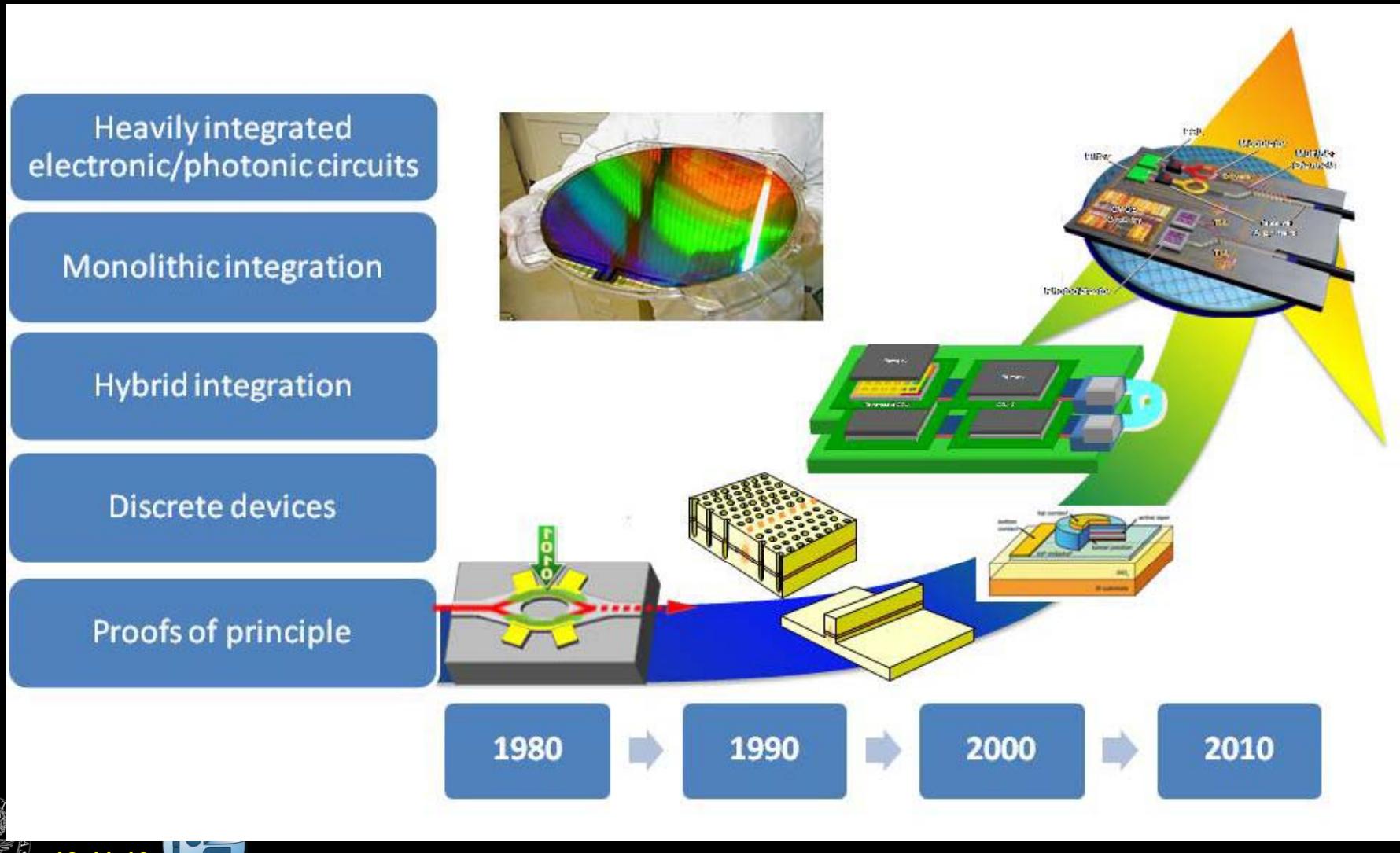
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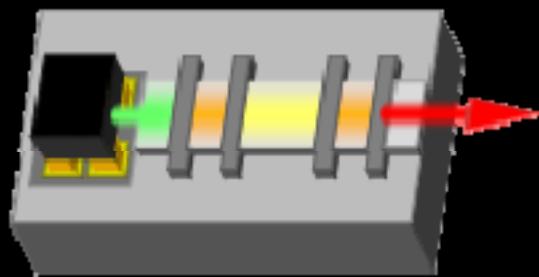


# Explosion of silicon photonics

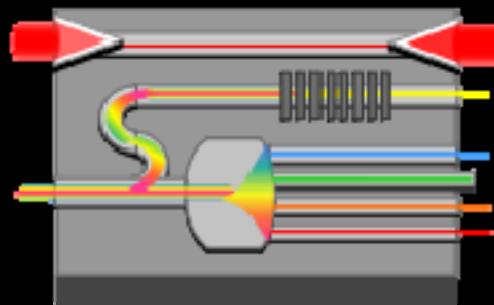


# From Building Block Research

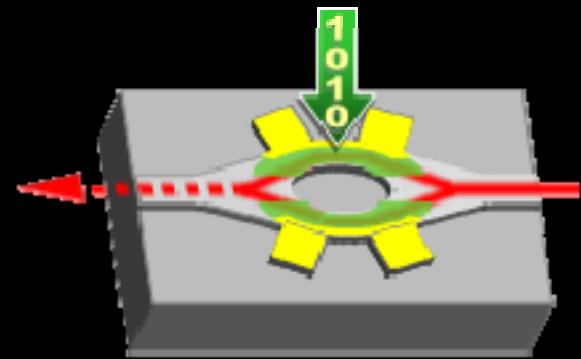
**1) Light Source**



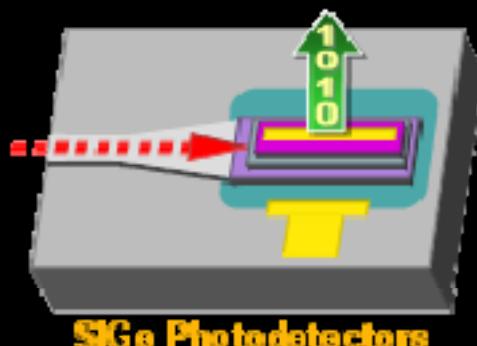
**2) Guide Light**



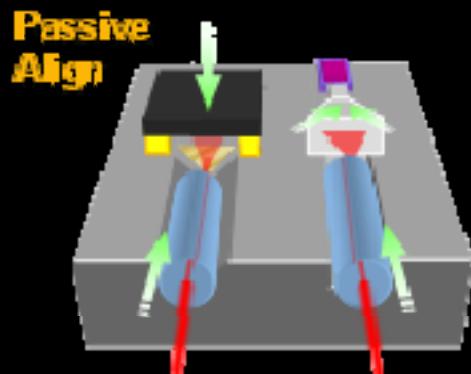
**3) Modulation**



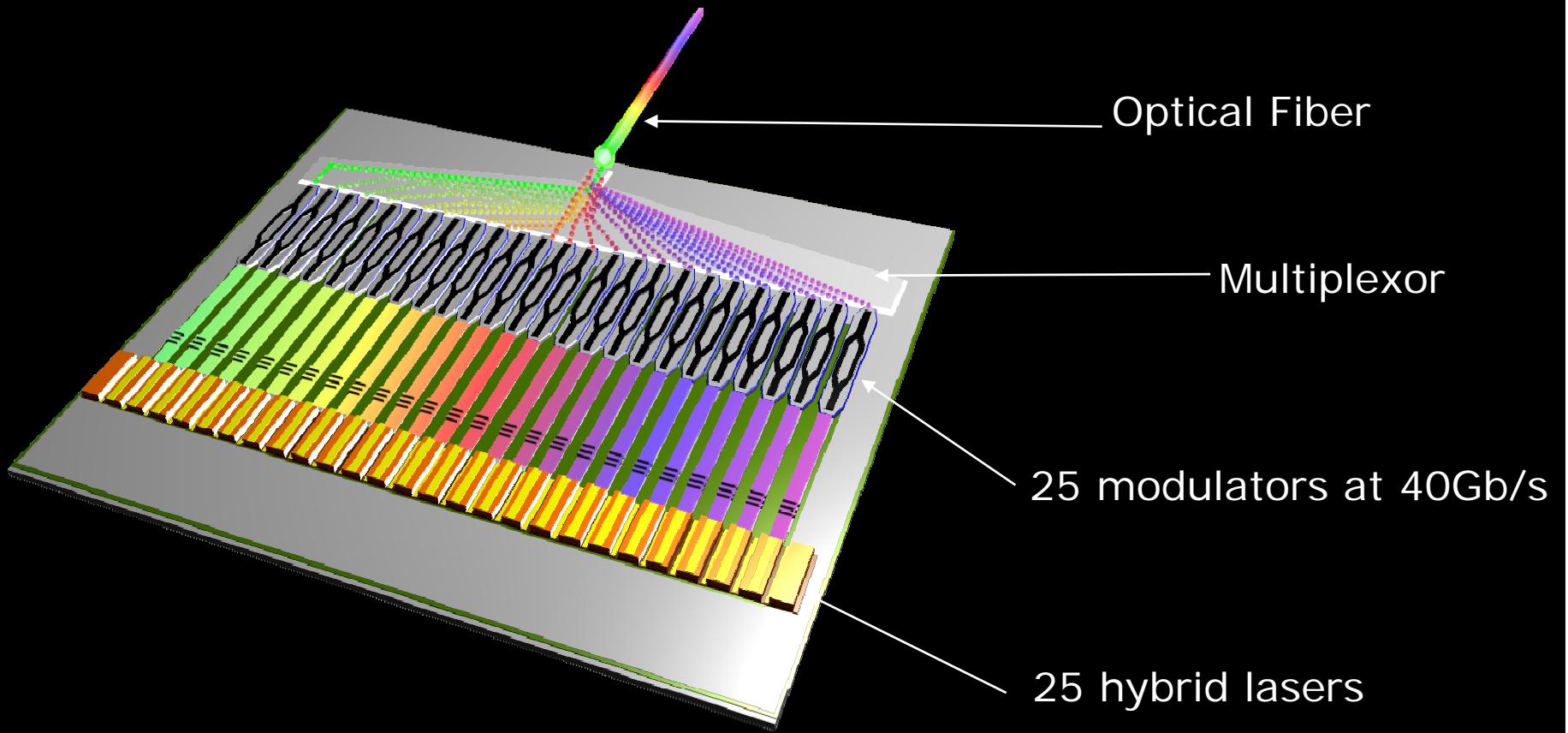
**4) Photo-detection**



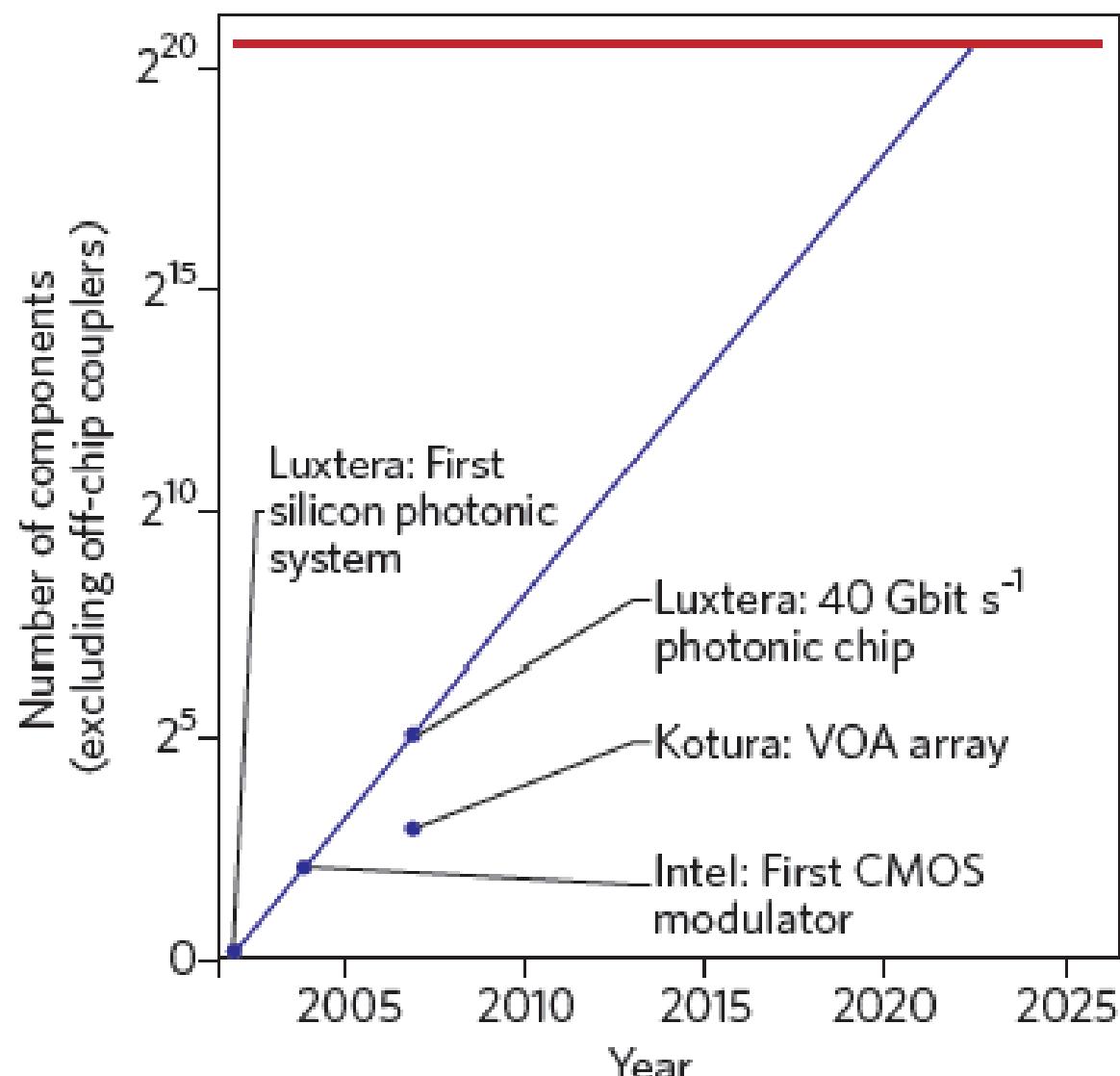
**5) Low Cost Assembly**



# To Large scale integration

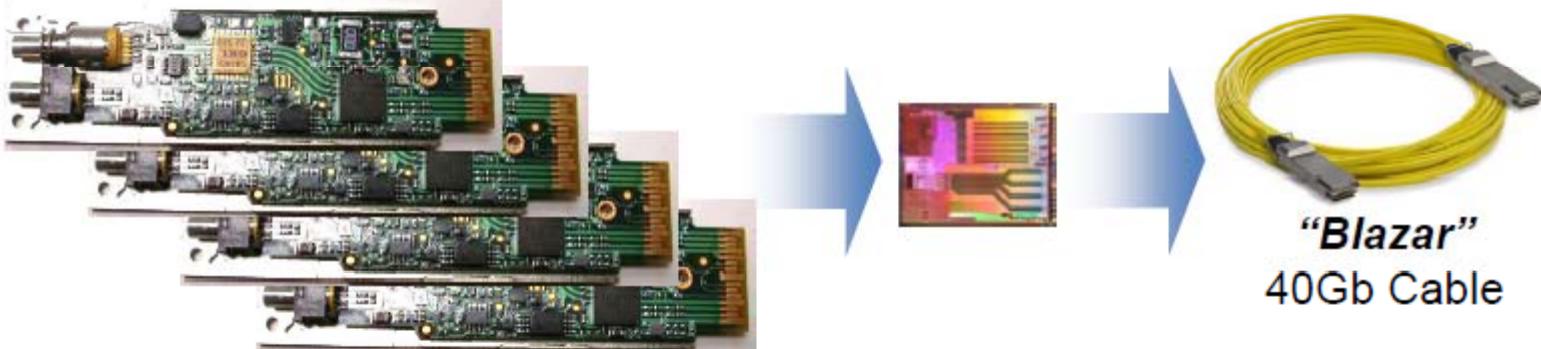


**A future integrated 1 Tb/s optical link  
on a single silicon chip**

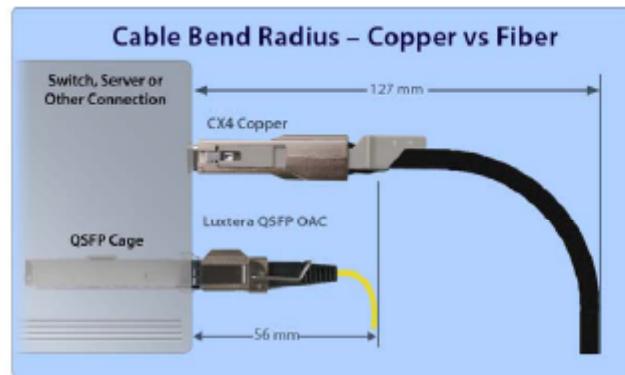


# CMOS Photonics Commercialization at Luxtera

Functionality of Four SFP+ 10Gb Transceivers on a single CMOS Die

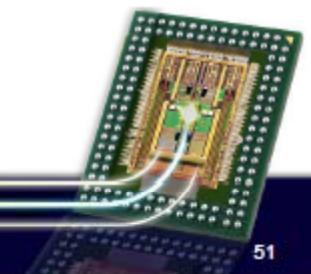


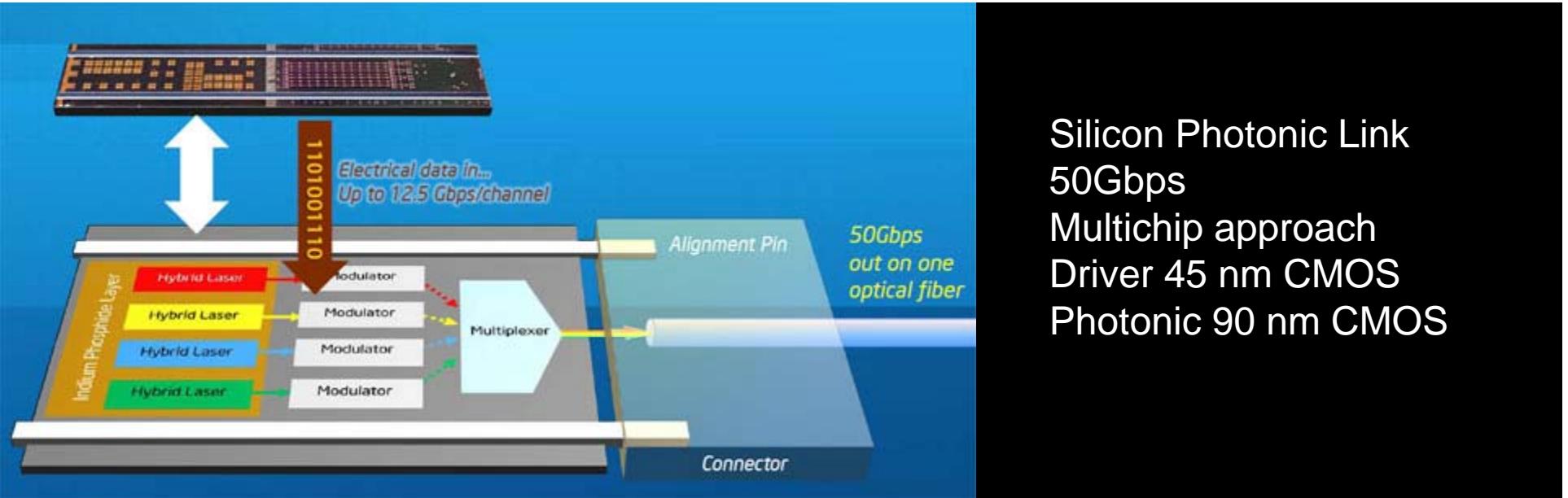
Optics is now price-competitive with copper!



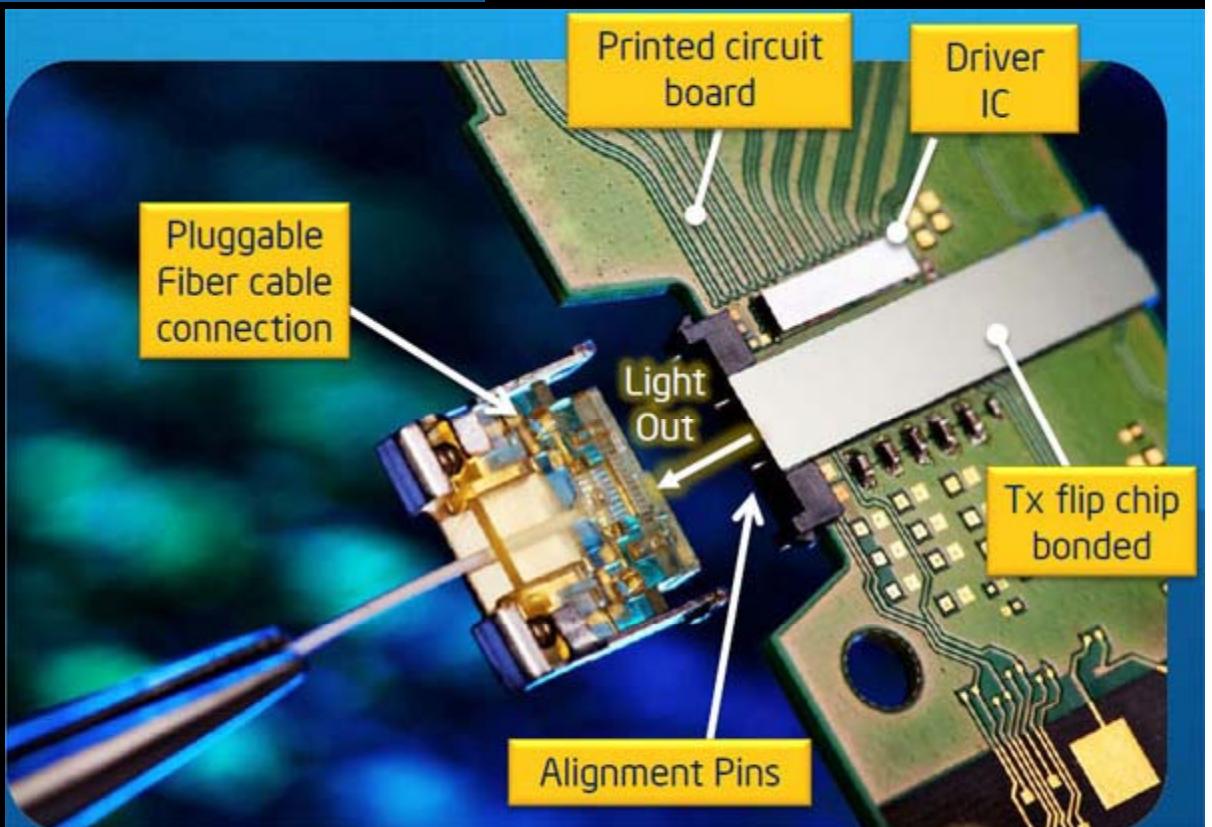
Benefits of optics maintained:

- 20% higher density
- 40% smaller bend radius
- 85% lighter cable
- 600% longer reach





Silicon Photonic Link  
50Gbps  
Multichip approach  
Driver 45 nm CMOS  
Photonic 90 nm CMOS



# Outline

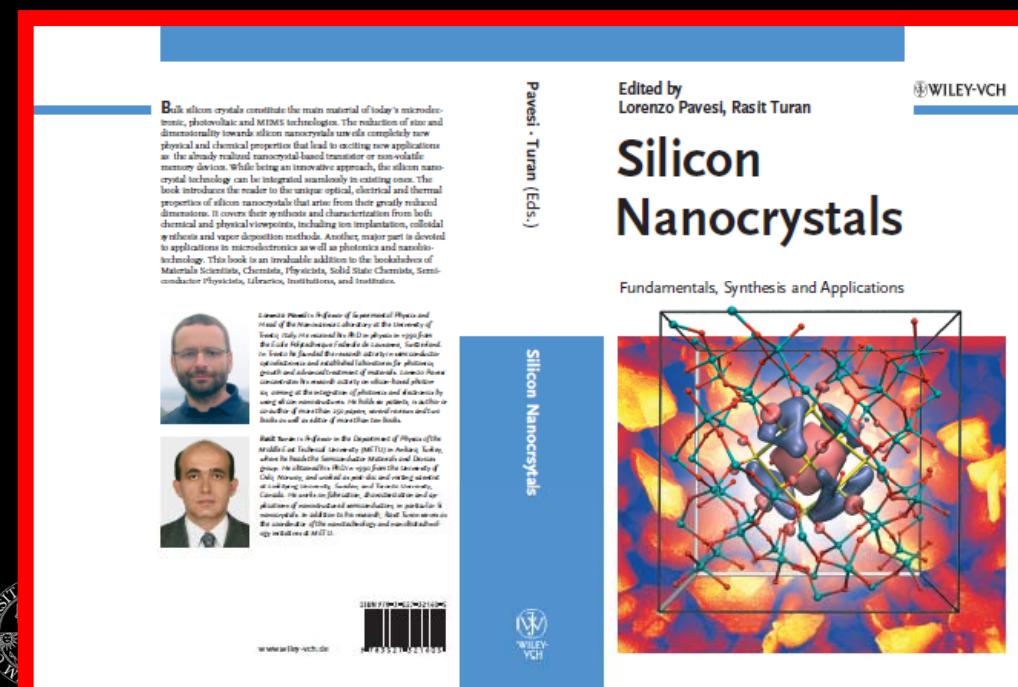
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# Nanosilicon photonics: a platform where silicon nanoclusters enable new functionalities in silicon photonics



508 Laser & Photonics  
Reviews

Laser & Photon. Rev. 3, No. 6, 508–534 (2009) / DOI 10.1002/lpor.200810045

**Abstract** Silicon photonics is no longer an emerging field of research and technology but a present reality with commercial products available on the market where low-dimensional silicon (nanosilicon or nano-Si) can play a fundamental role. After a brief history of the field, the optical properties of silicon reduced to nanometric dimensions are introduced. The use of nano-Si in the form of Si nanocrystals, in the main building blocks of silicon photonics (waveguides, modulators, sources and detectors) is reviewed and discussed. Recent advances of nano-Si devices such as waveguides, optical resonators (linear, ring, and disk) are treated. Emphasis is placed on the unique optical gain properties of nano-Si and the sensitization effect on Er ions to achieve infrared light amplification. The possibility of electrical injection in light-emitting diodes is presented as well as recent attempts to exploit nano-Si for solar cells. In addition, nonlinear optical effects that will enable fast all-optical switches are described.

**Si-nc** A schematic diagram showing several green circles labeled 'Si-nc' containing a central red star labeled 'Er3+'. Blue arrows point from the 'Er3+' centers towards the outer edges of the green circles, indicating the sensitization process.

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## Nanosilicon photonics

Nicola Daldosso\* and Lorenzo Pavesi  
Nanoscience Laboratory, Physics Department, University of Trento via Sommarive 14, 38050 Povo (Trento), Italy

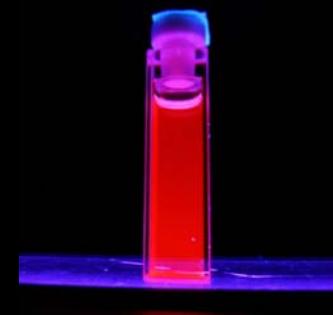
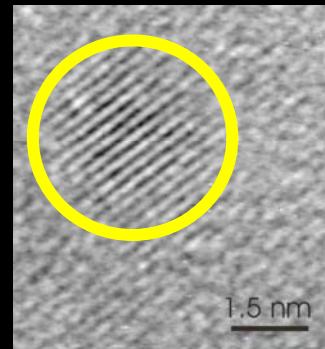
Received: 25 August 2008, Revised: 6 February 2009, Accepted: 11 March 2009  
Published online: 2 June 2009

**Key words:** Nanosilicon, photonics, optical amplification, non-linear properties.

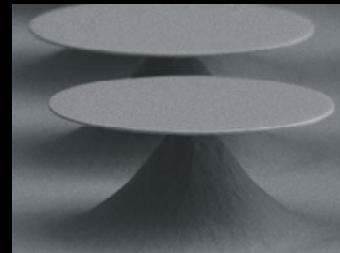
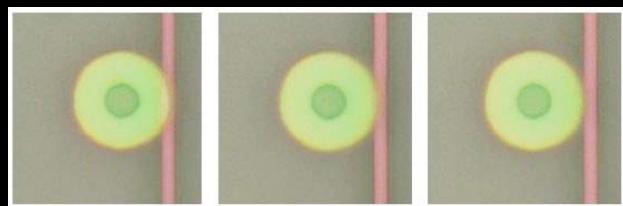
**PACS:** 42.62.-b, 42.65.-k, 78.67.Bf, 81.07.-b, 85.60.-q

# Silicon Nanophotonics

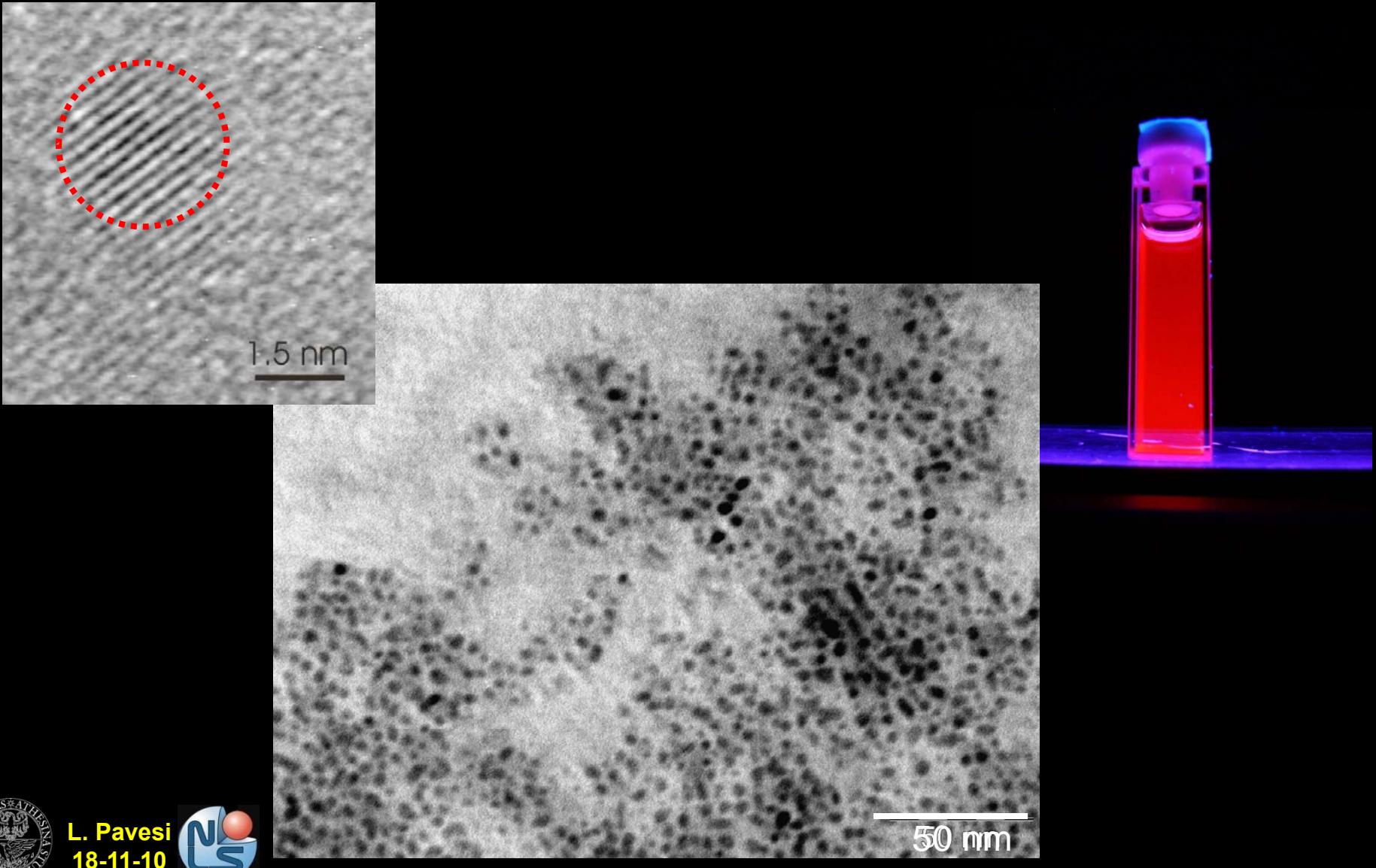
- Confine carriers on nanoscale dimensions



- Confine photons on nanoscale dimensions



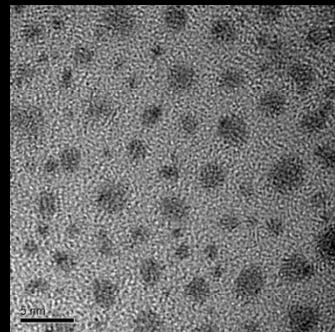
# Silicon quantum dots



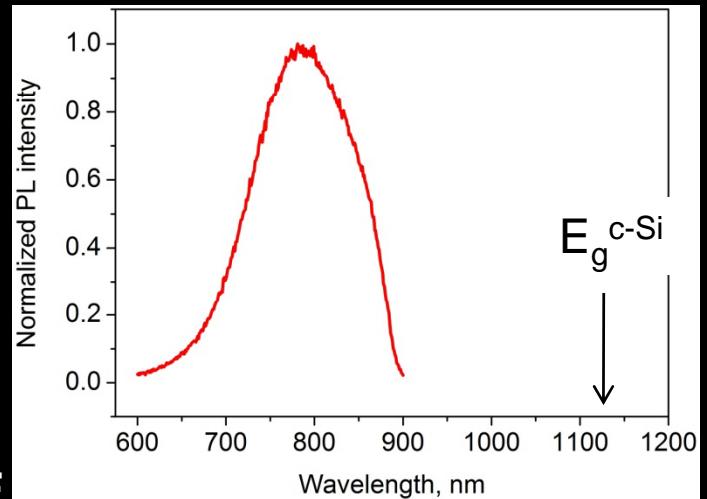
# Silicon quantum dots



**Bulk Silicon:**  
Indirect band-gap  
  
inefficient light emitter



**Nanocrystalline-Si:**  
Direct-gap due to QCE  
Strong visible light  
emission



## Optical gain in silicon nanocrystals

L. Pavesi\*, L. Dal Negro\*, C. Mazzoleni\*, G. Franzò† & F. Priolo†

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440



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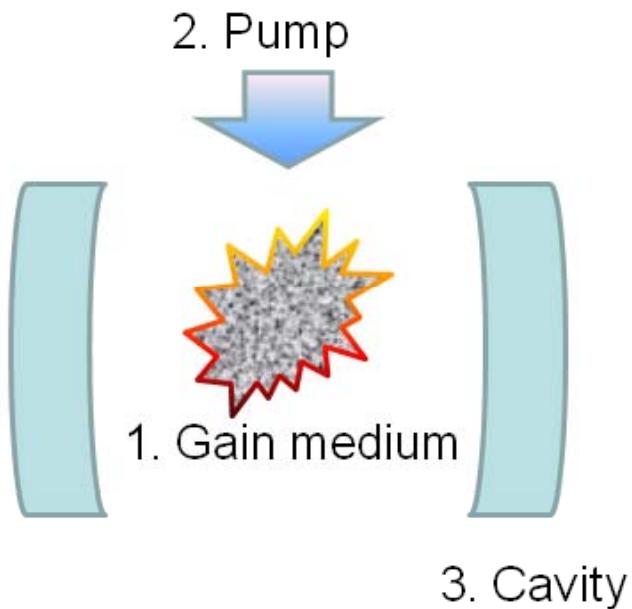


# Optical gain in silicon nanocrystals

L. Pavesi\*, L. Dal Negro\*, C. Mazzoleni\*, G. Franzò† & F. Priolo†

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→ Silicon laser ?

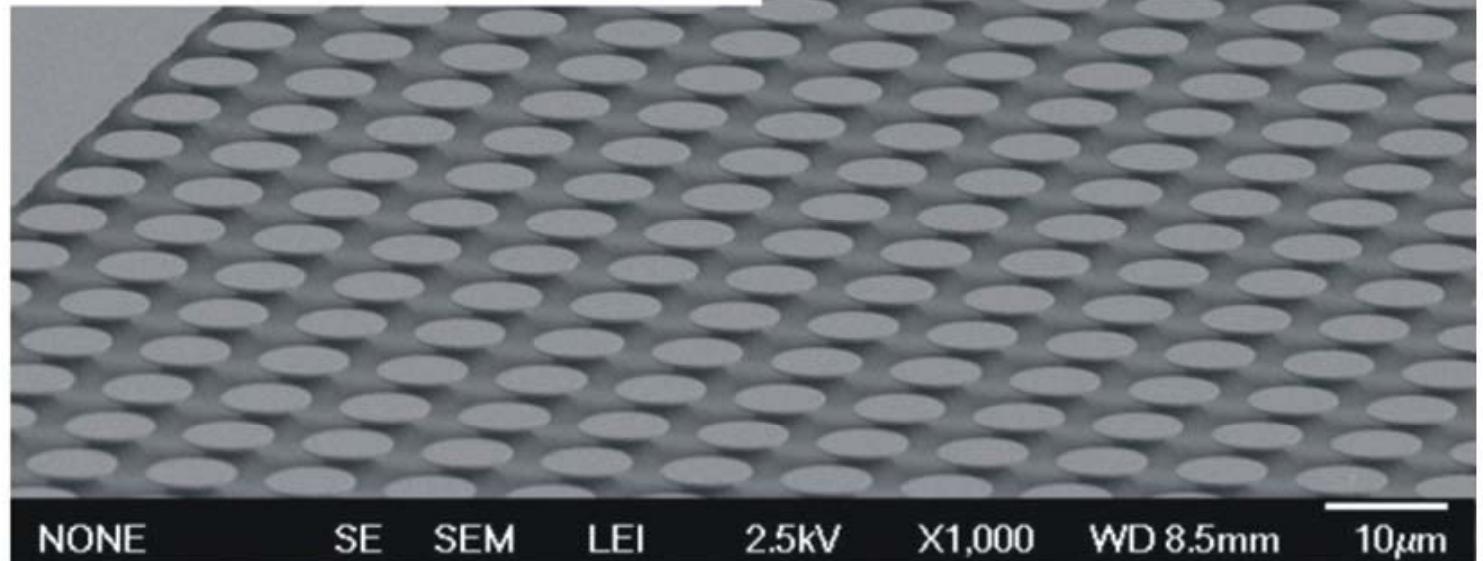
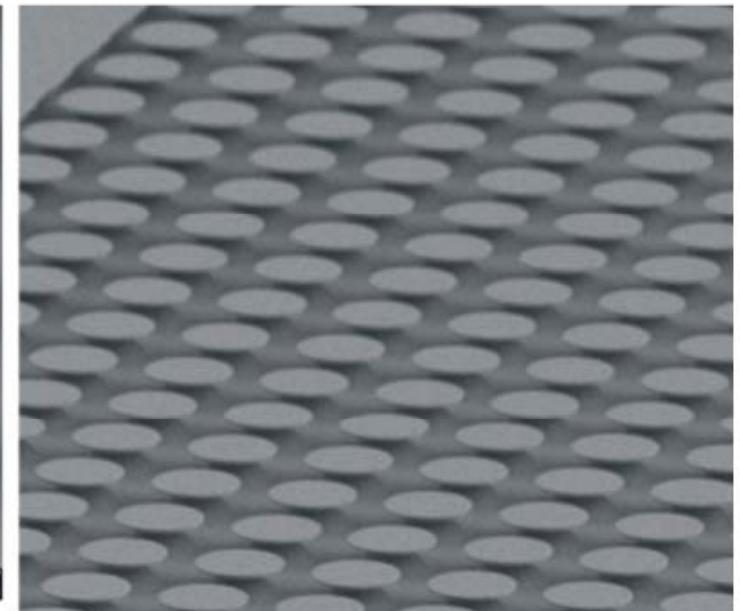
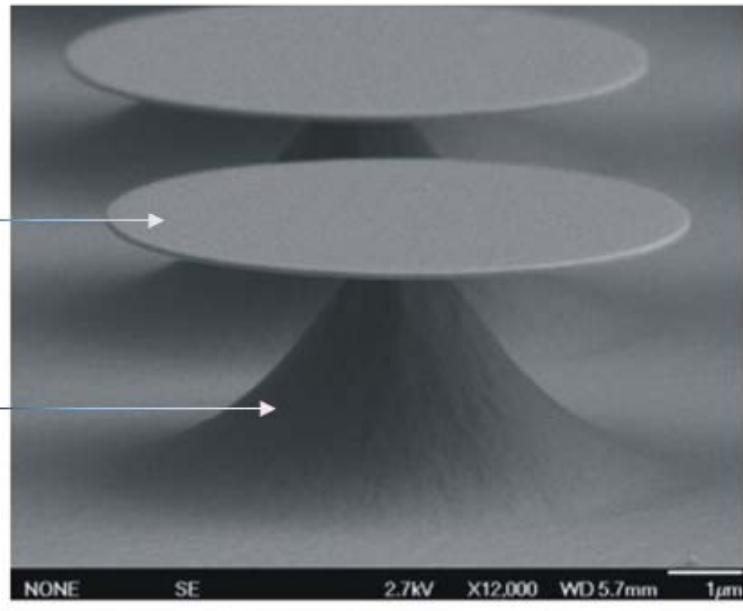


e.g., a **Whispering-gallery mode resonator**

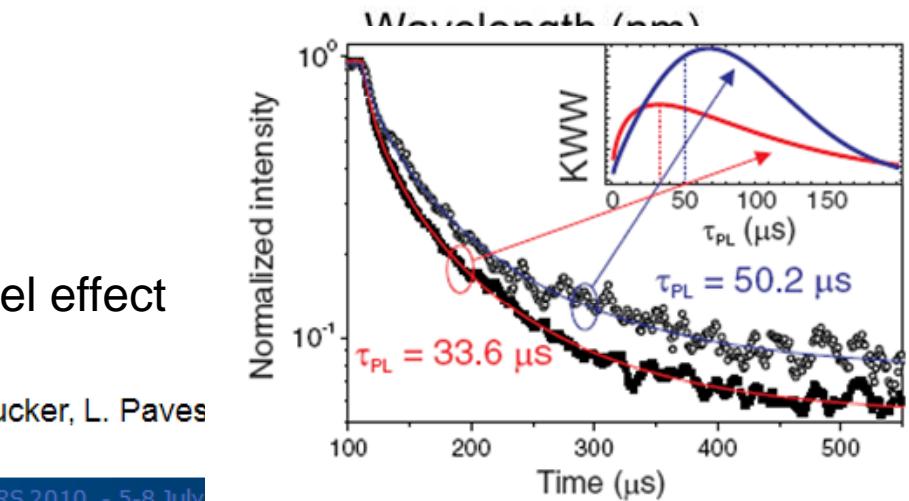
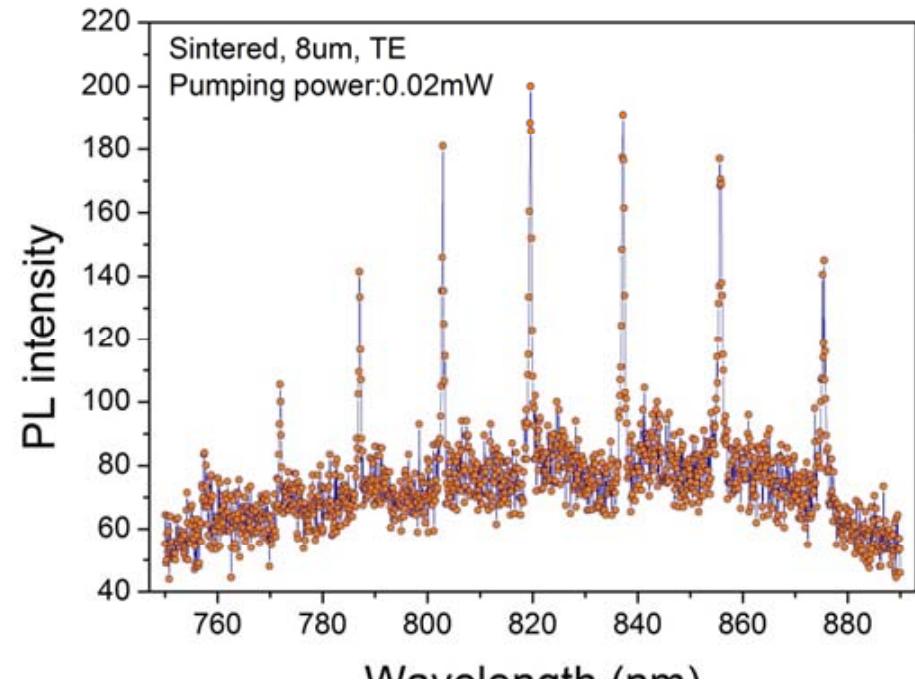
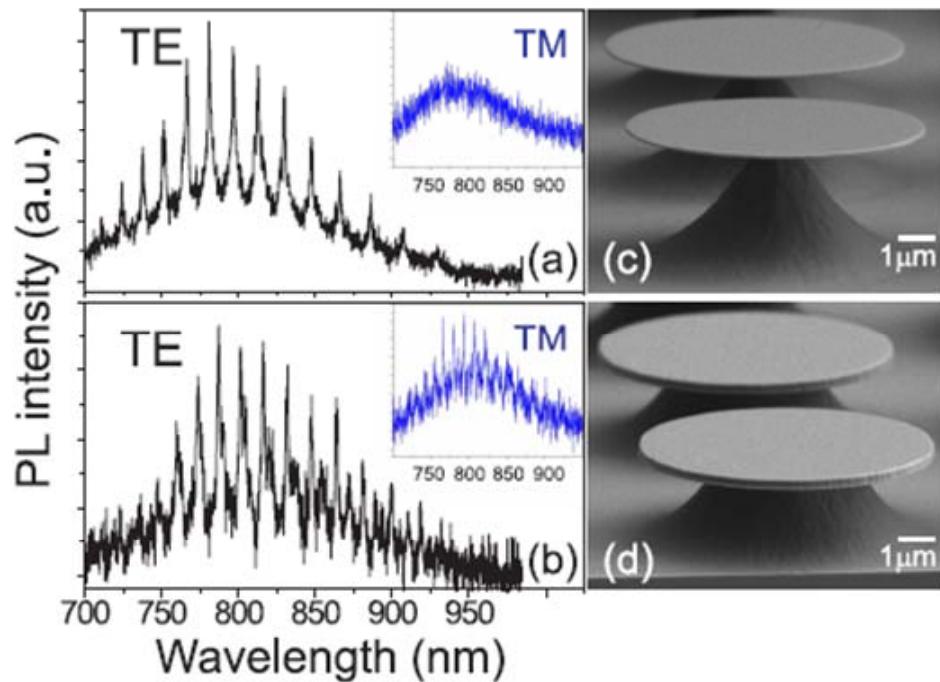
## Si QD's in 2D whispering-gallery resonators

Si-nc/SiO<sub>2</sub>

c-Si



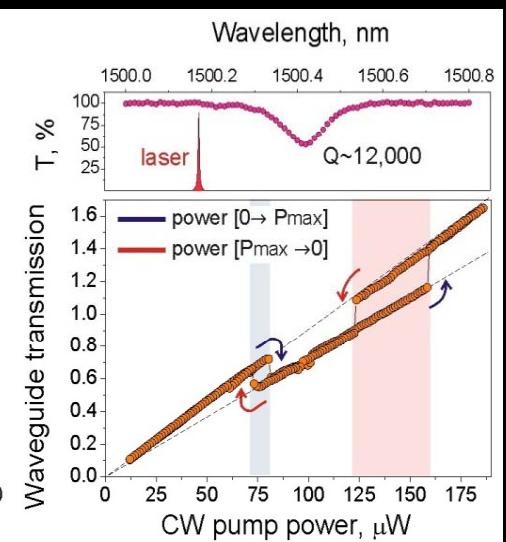
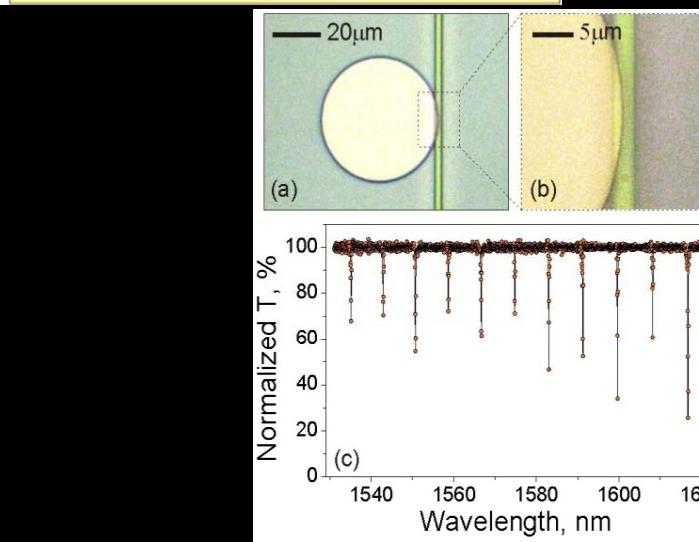
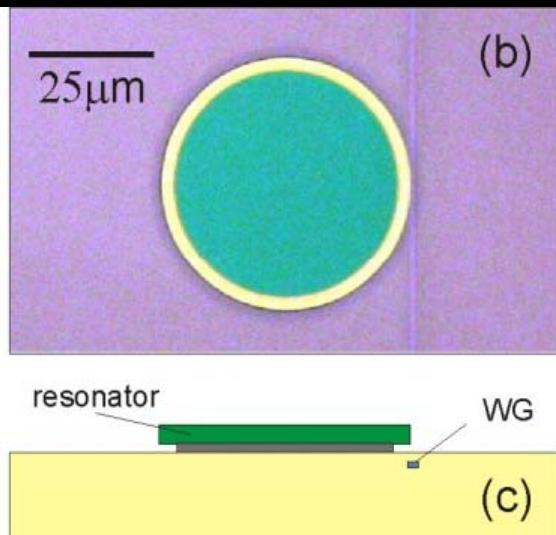
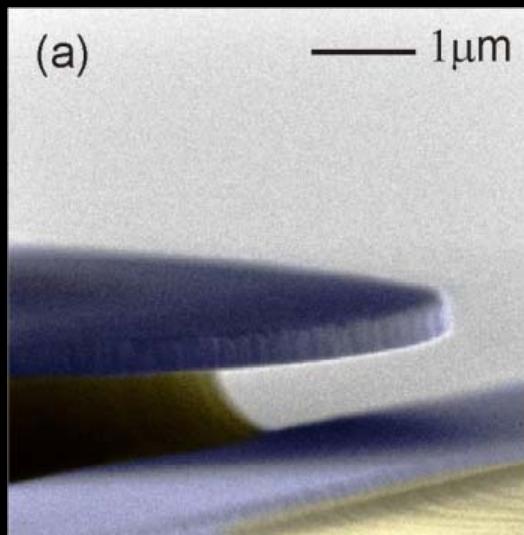
## Si QD's in 2D whispering-gallery resonators



Purcel effect

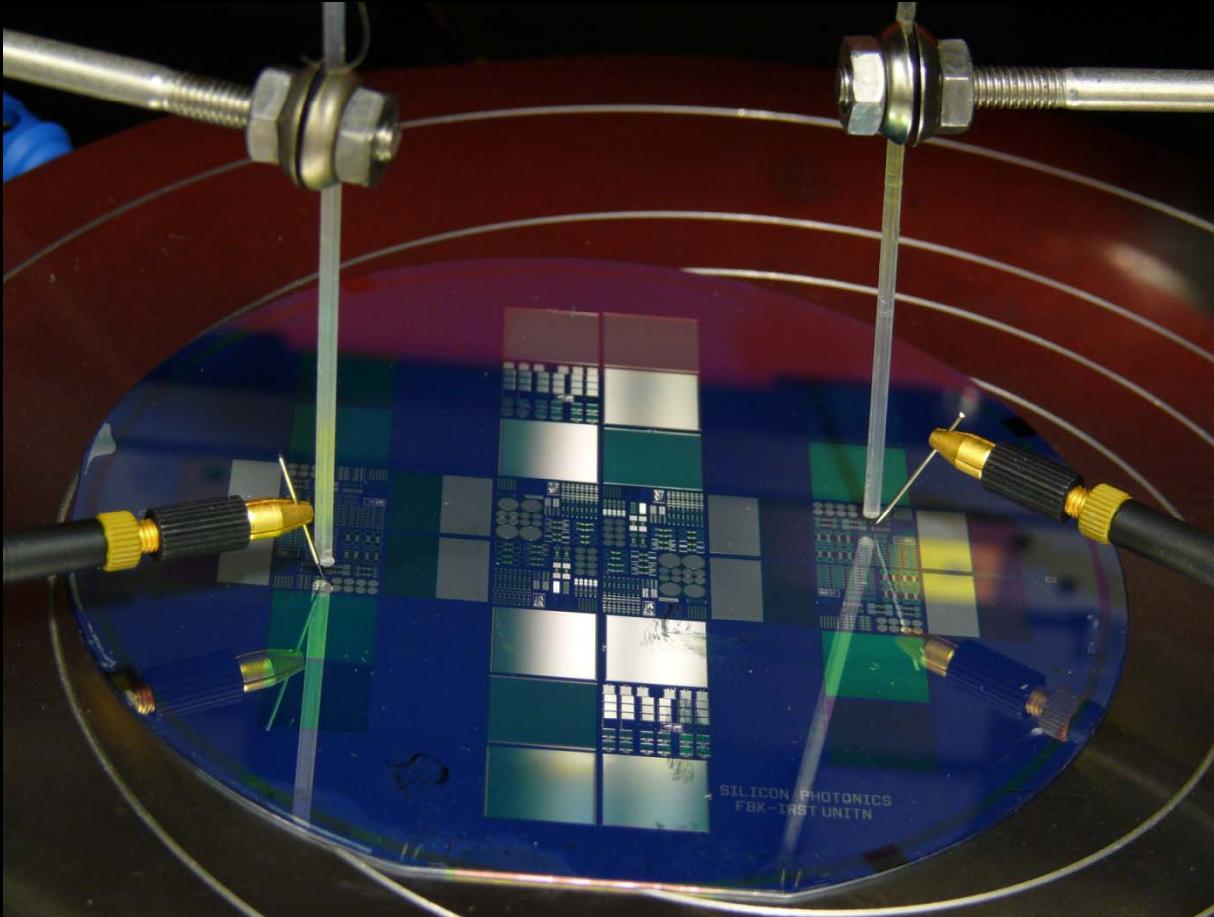
M. Ghulinyan, D. Navarro-Urrios, A. Pitanti, Alberto Lui, Georg Pucker, L. Paves  
OPT. EXPRESS 16, 13218-13224 (2008)

# Integration of microdisk with a waveguide



THE all SILICON TRANSCEIVER

# *pHotonics EElectronics functional Integration on CMOS*



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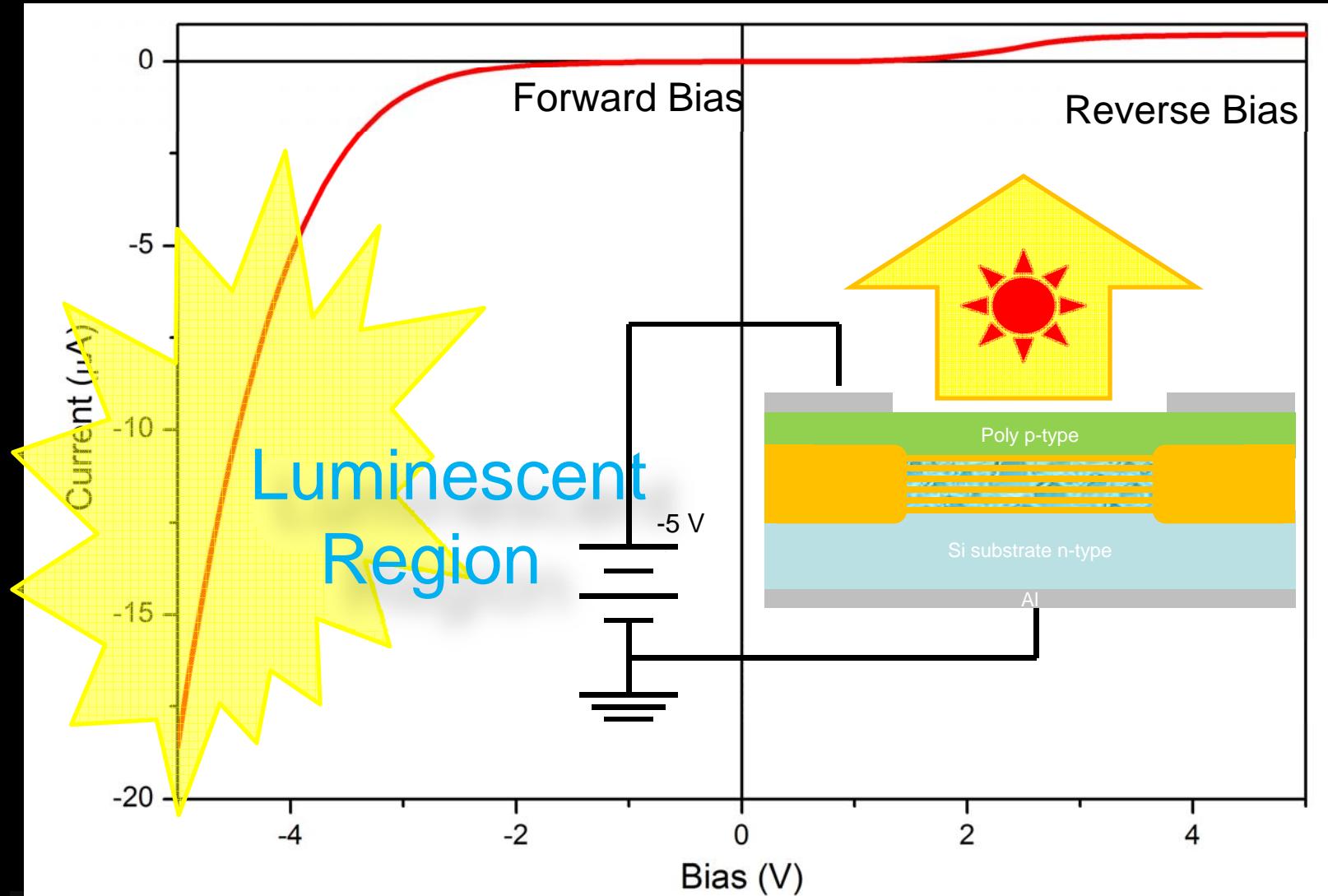


Marconi, Anopchenko

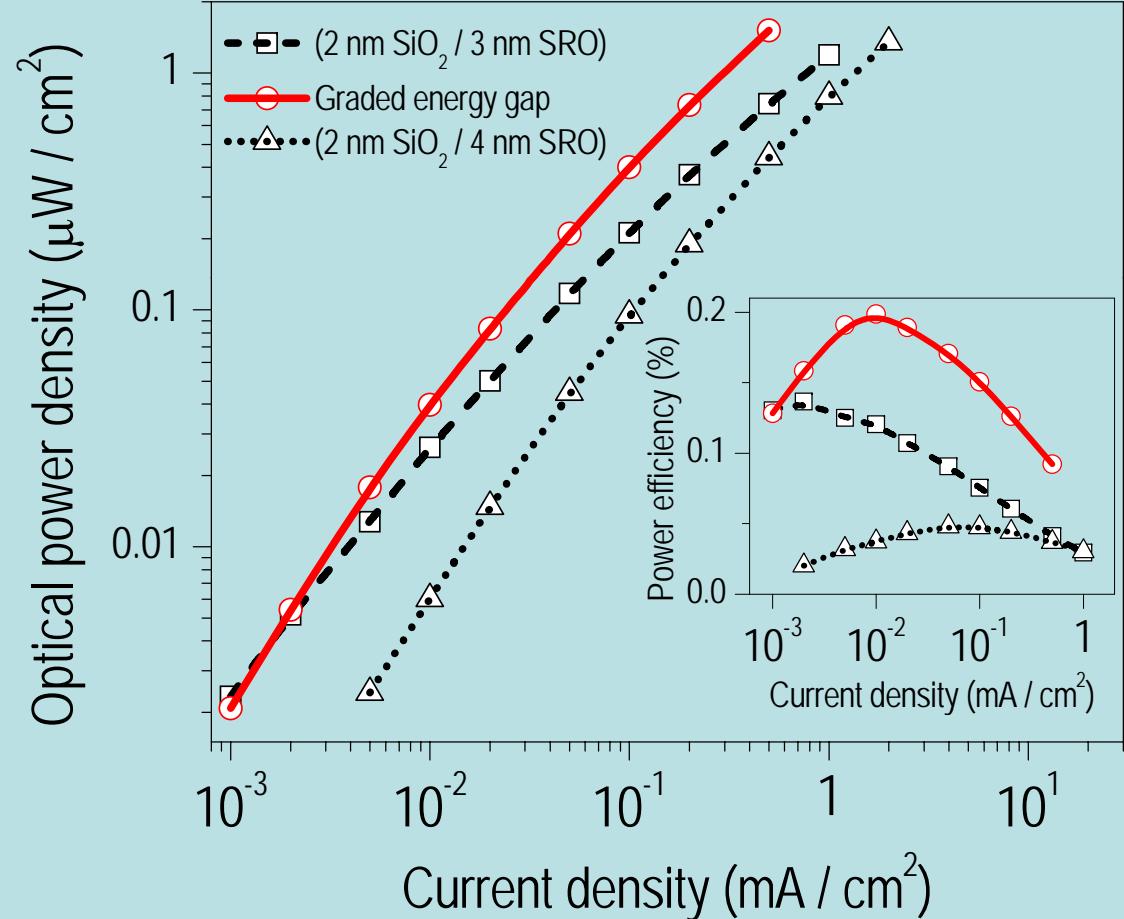
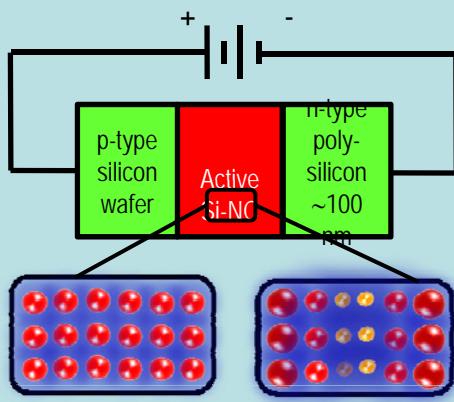
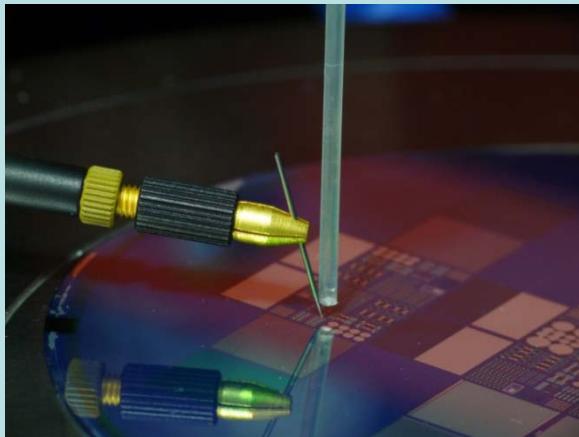


# THE all SILICON TRANSCEIVER

## *p*Hotonics EElectronics functional Integration on CMOS

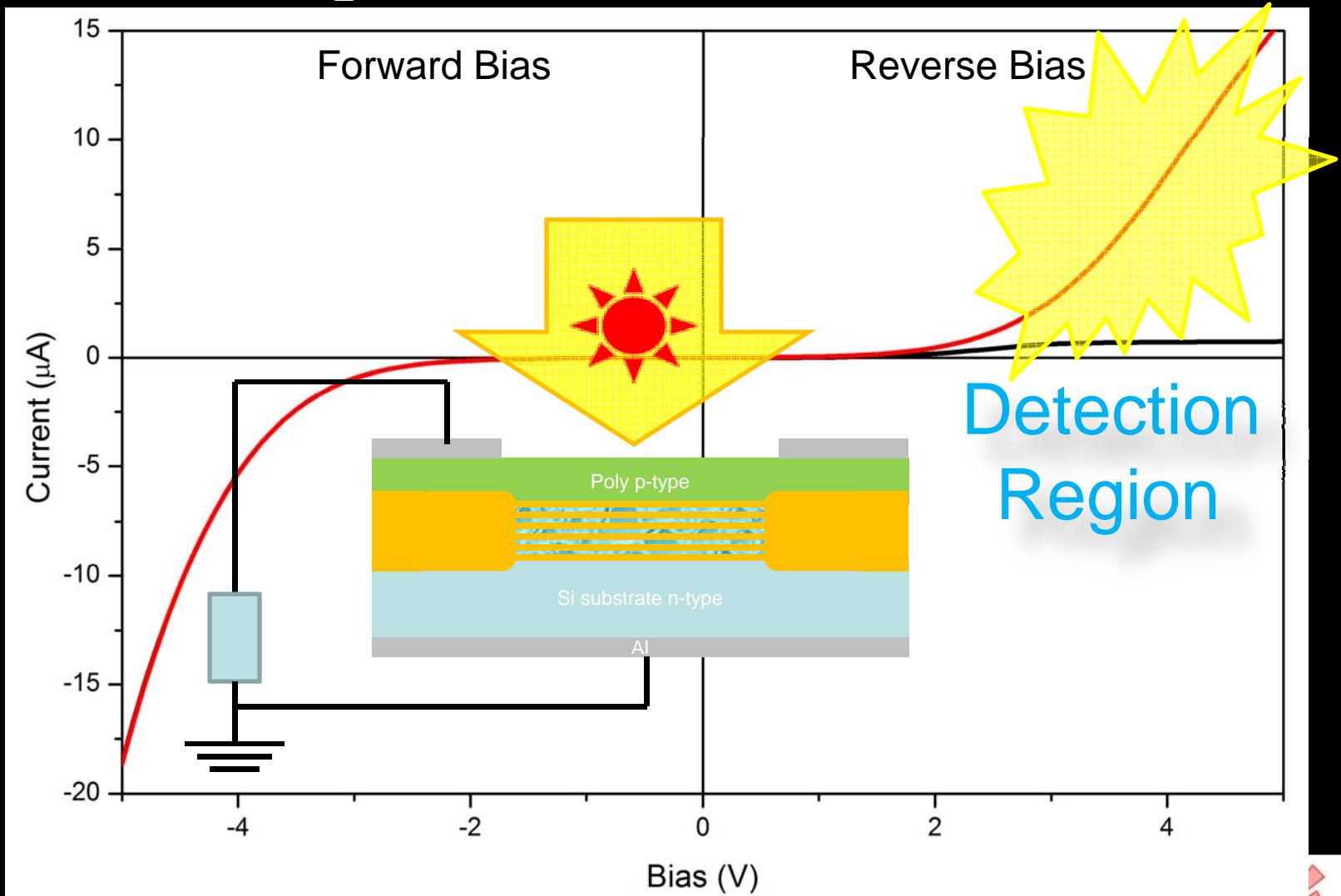


# *p*hotronics *E*lectronics functional Integration on CMOS

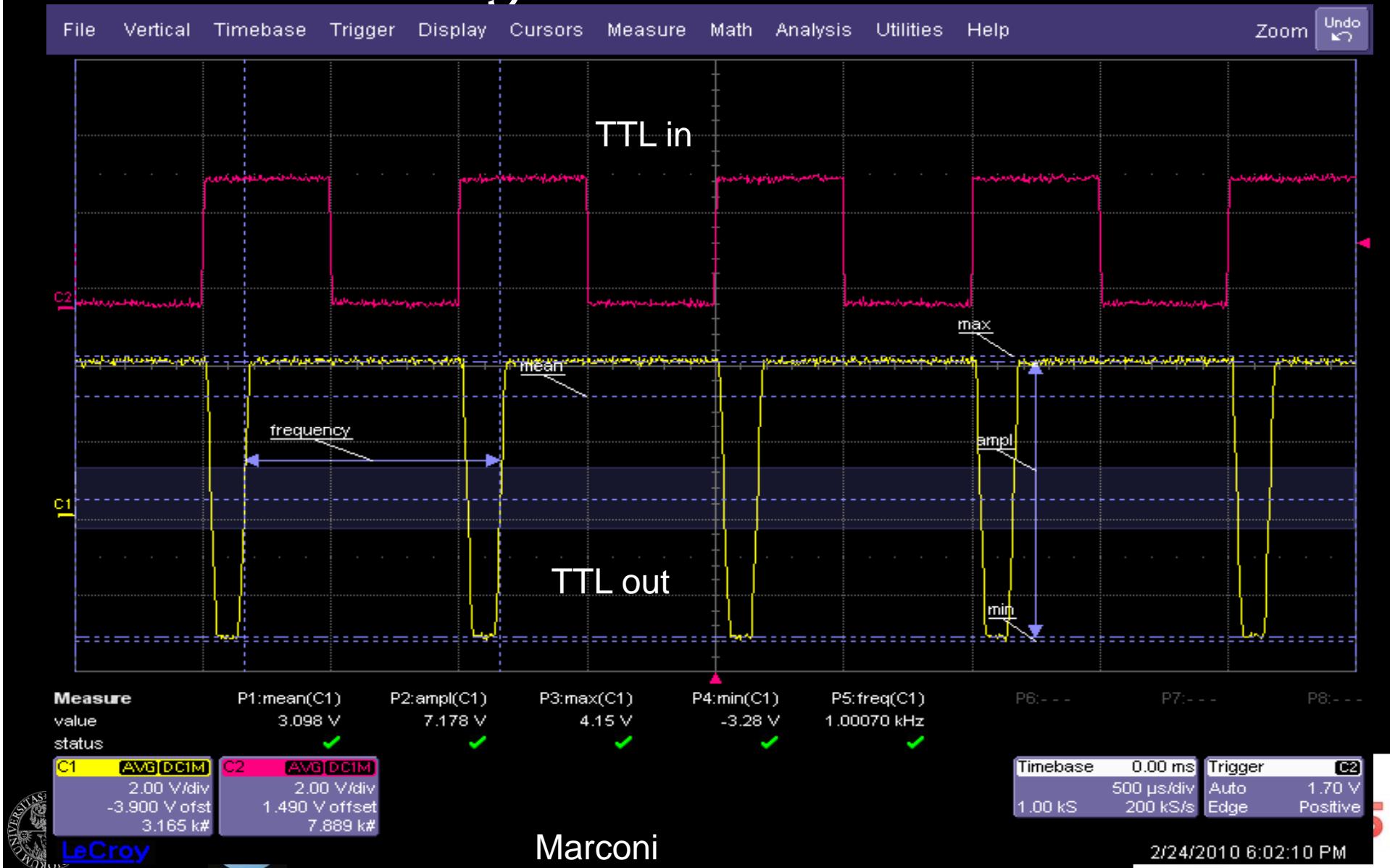


# THE all SILICON TRANSCEIVER

## *p*Hotonics EElectronics functional Integration on CMOS



# *p*Hotonics EElectronics functional Integration on CMOS



# All optical switching with silicon nanocrystals

$$n = n_0 + n_2 |I|$$

$$\alpha = \alpha_0 + \beta |I|$$

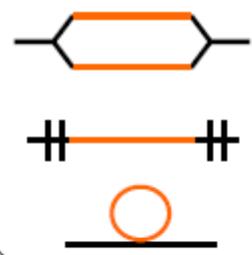


Refractive index variation

Effective index variation of the  
guided optical mode



Interferometers



Phase variation



Optical intensity  
variation

# Comparison to other nonlinear materials

Silica



$$n_2 = (1.54 \times 10^{-16}) \text{ cm}^2/\text{W} [3,4]$$

Bulk Silicon



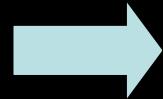
$$n_2 = (4.5 \times 10^{-14}) \text{ cm}^2/\text{W} [3,4]$$

GaAs



$$n_2 = (1.59 \times 10^{-13}) \text{ cm}^2/\text{W} [5]$$

Si-ncs



$$n_2 = (2 \div 8 \times 10^{-13}) \text{ cm}^2/\text{W} [\text{present work}]$$

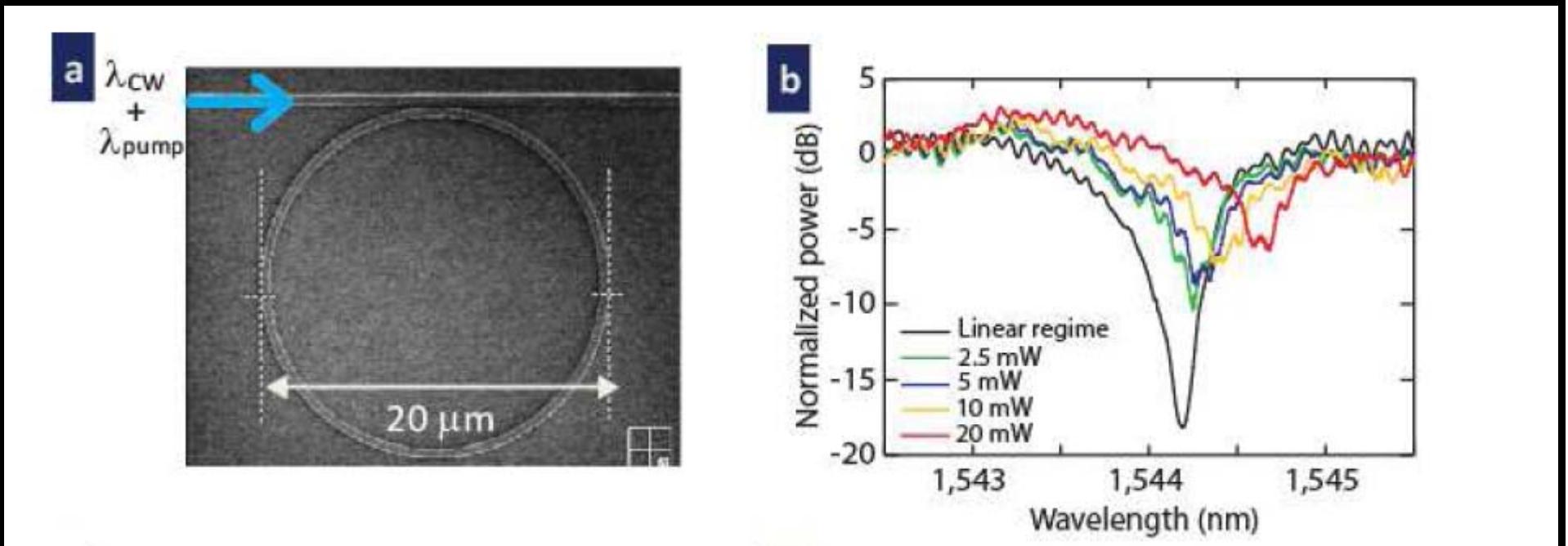
[3] Handbook of Nonlinear Optics

[4] Adair R. et al., Physical Review B, 39, 3337, (February 1989).

[5] M. Dinu et al., Applied Physics Letters, 82, 2954 (2003).



# All optical switching



## Si nanocrystals activated slot waveguides

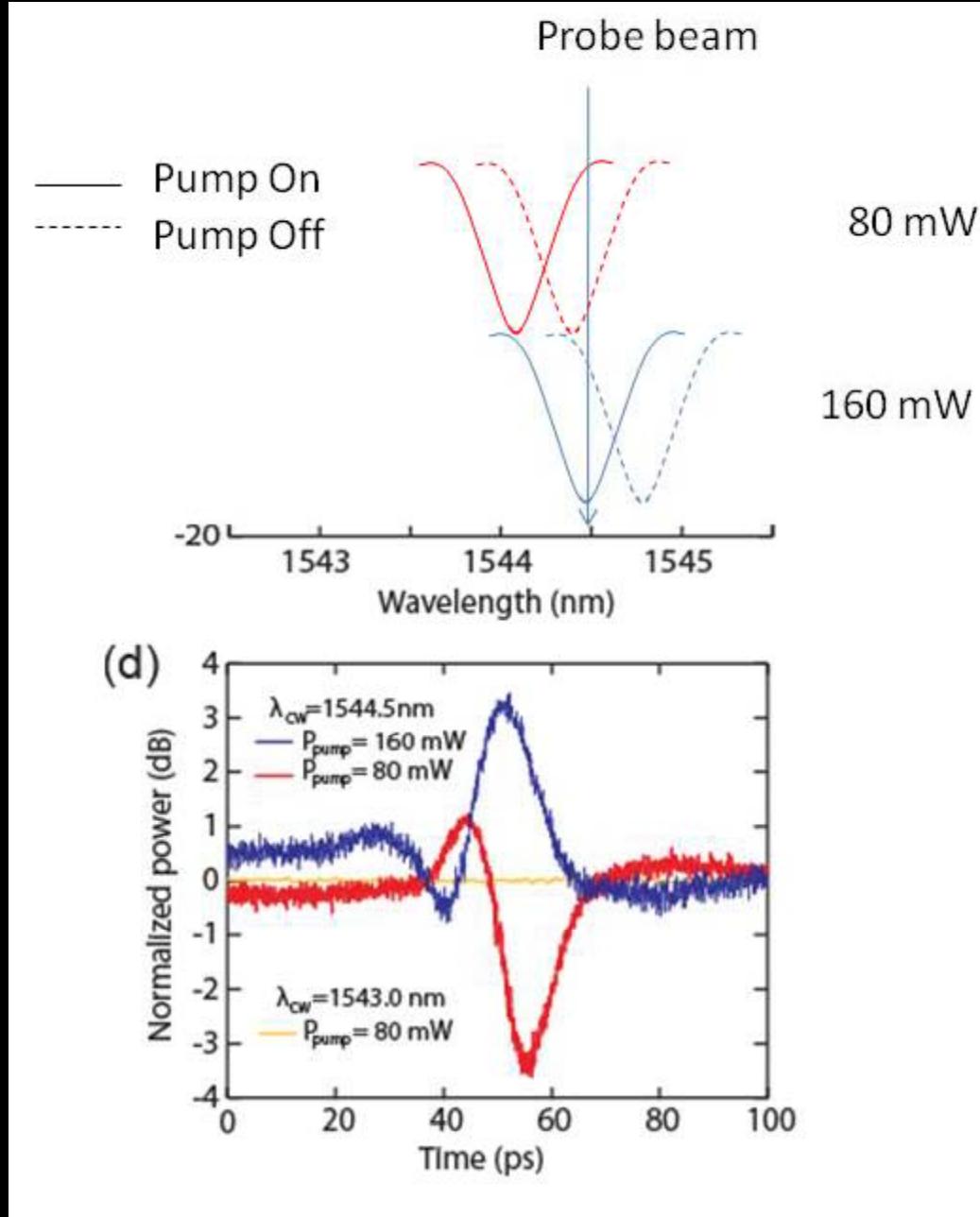


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A. Martinez et al. Nanoletters (2010)





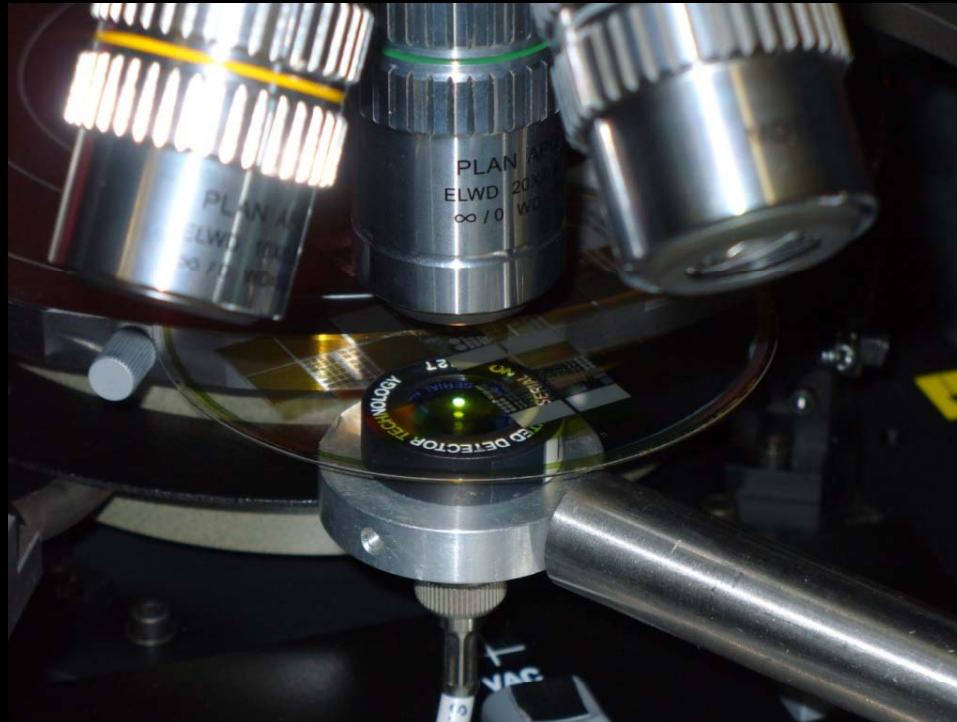
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A. Martinez et al. Nanoletters (2010)



# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*



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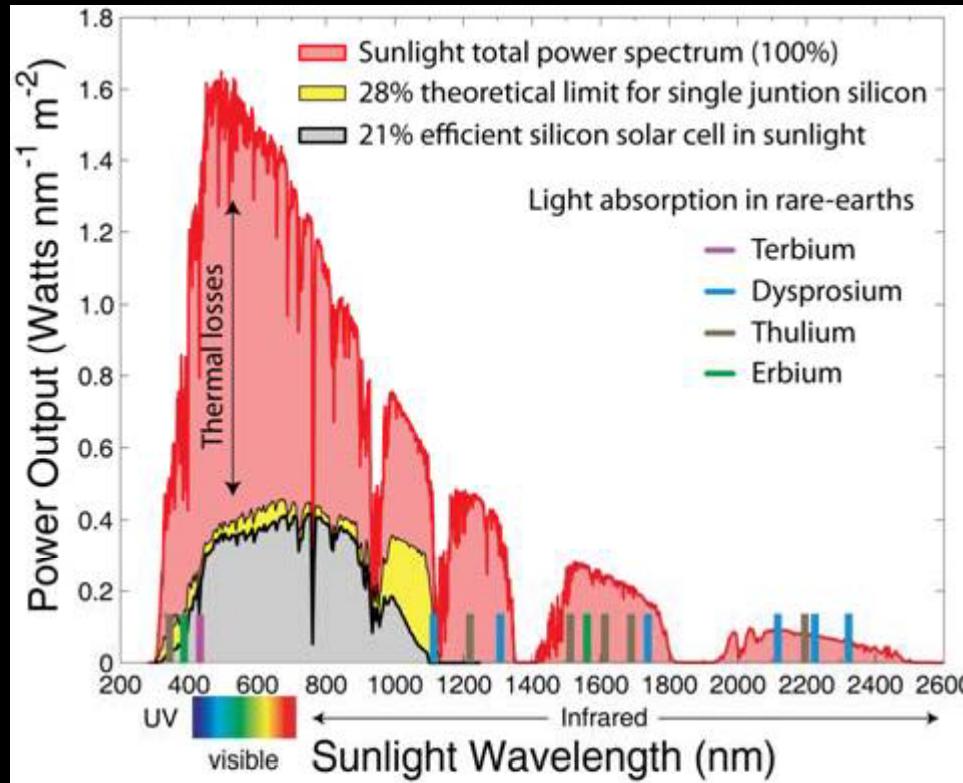


# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*

|  |              |
|--|--------------|
| <b>Photon electron energy conversion</b> | <b>32.9%</b> |
| Unabsorbed energy loss                   | 18.7%        |
| Heat loss                                | 46.8%        |
| Other losses                             | 1.6%         |



# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*

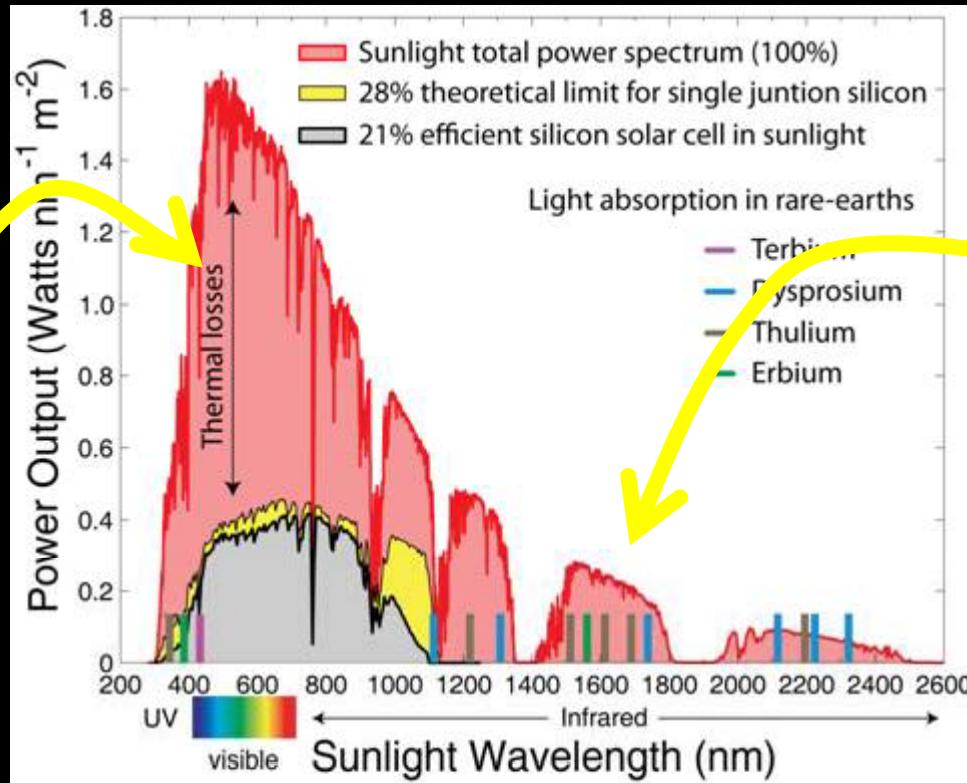


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# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*

downshifter



Secondary carrier generation



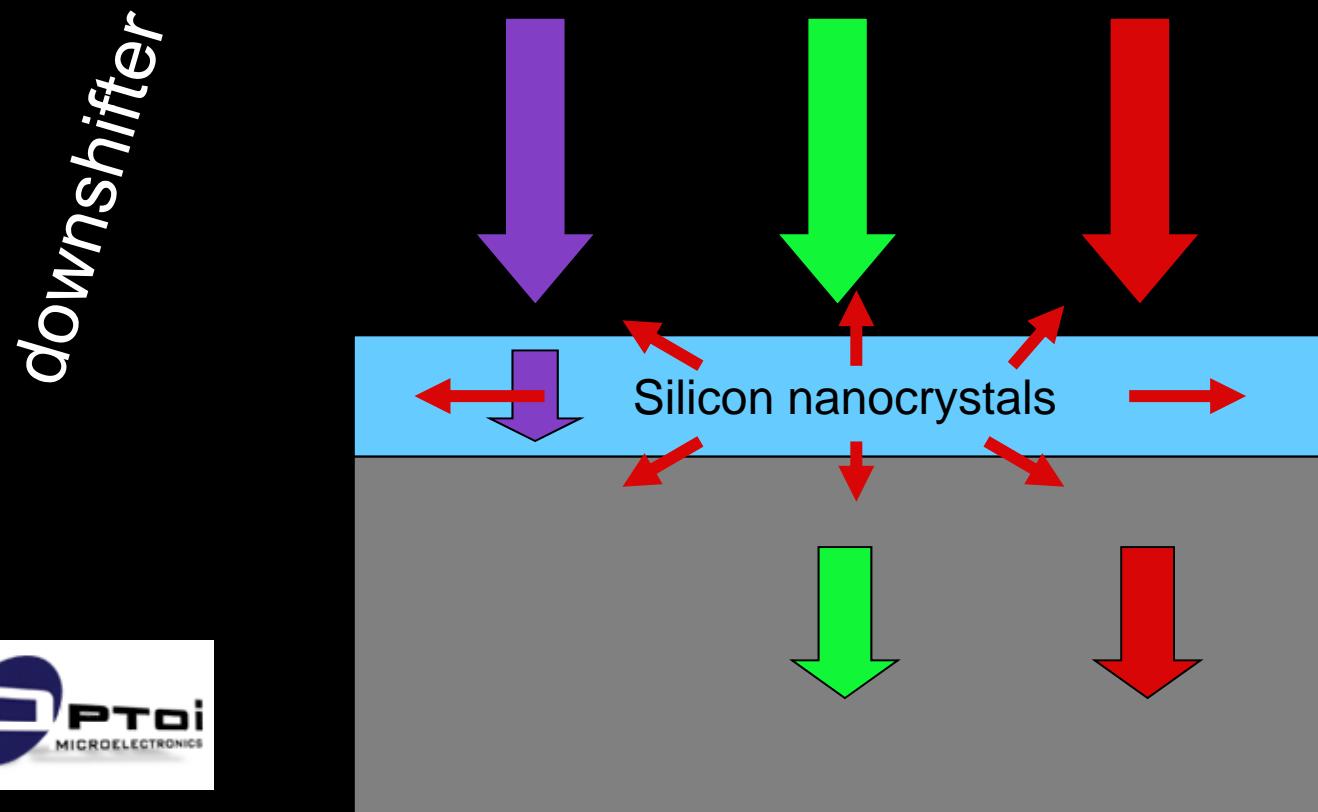
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# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*



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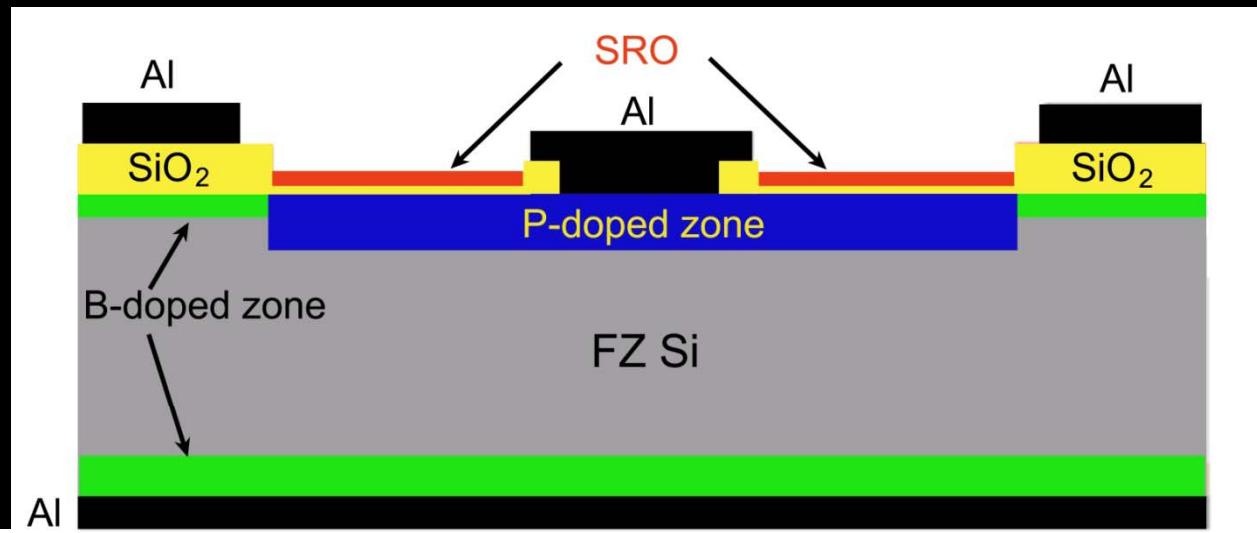


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# *Improved photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*

downshifter

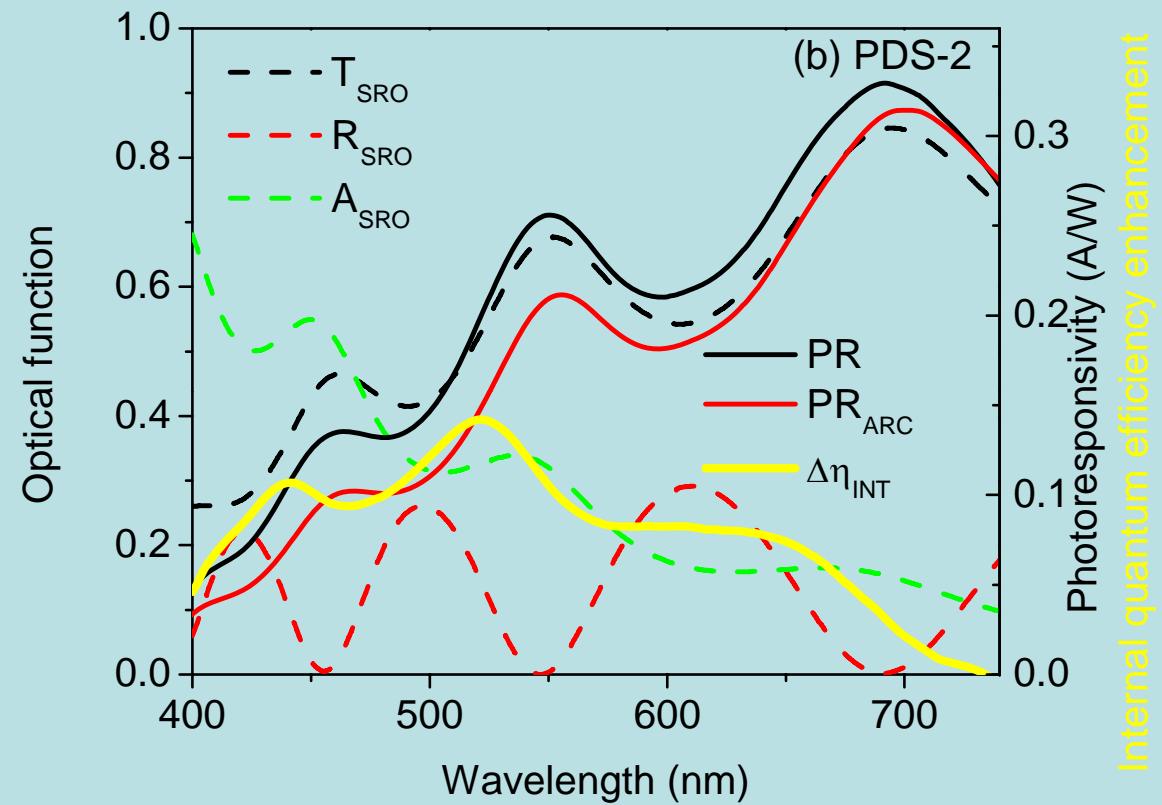


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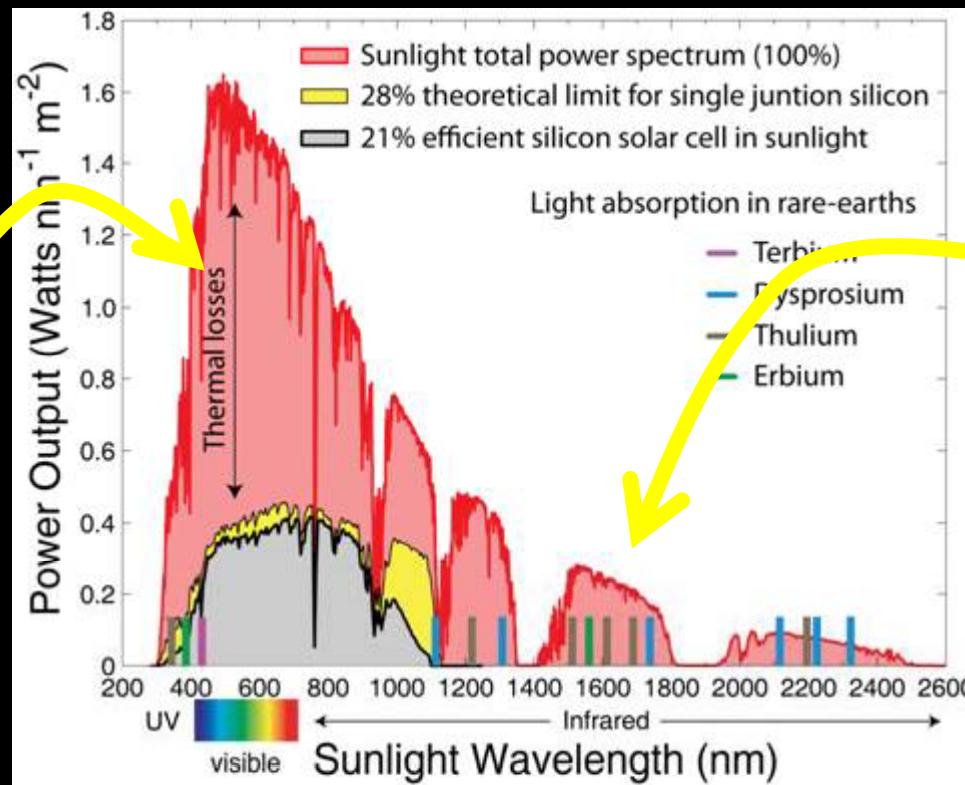


A maximum enhancement of the internal quantum efficiency of 14%



# *Improve photovoltaic efficiency by applying novel effects at the limits of light-matter interaction*

downshifter



Secondary carrier generation



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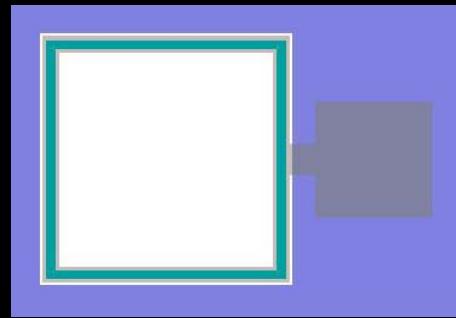
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## Cross section of the device



Device area = 320  $\mu\text{m}$  X 320  $\mu\text{m}$



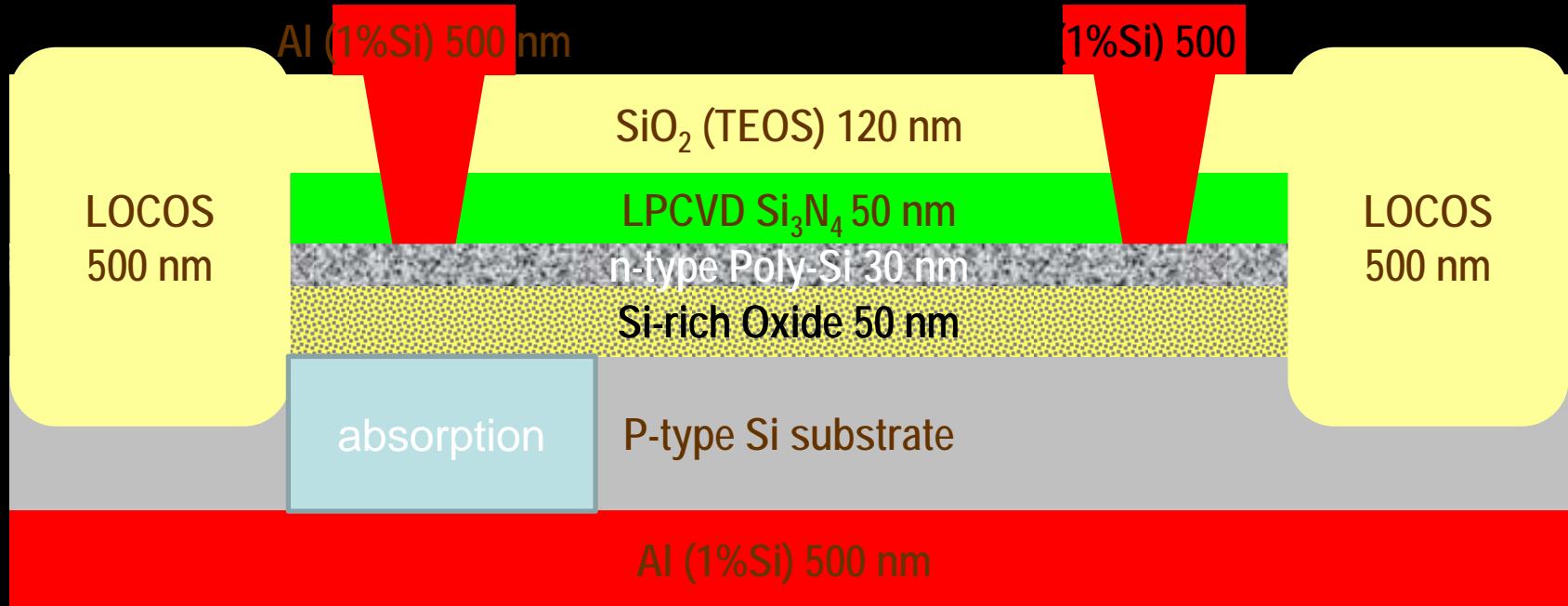
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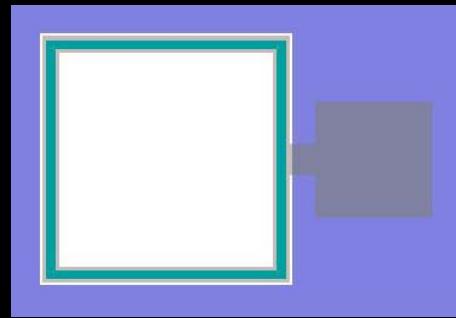
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## Cross section of the device



Device area = 320  $\mu\text{m} \times 320 \mu\text{m}$



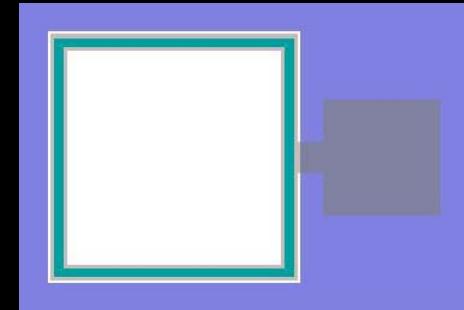
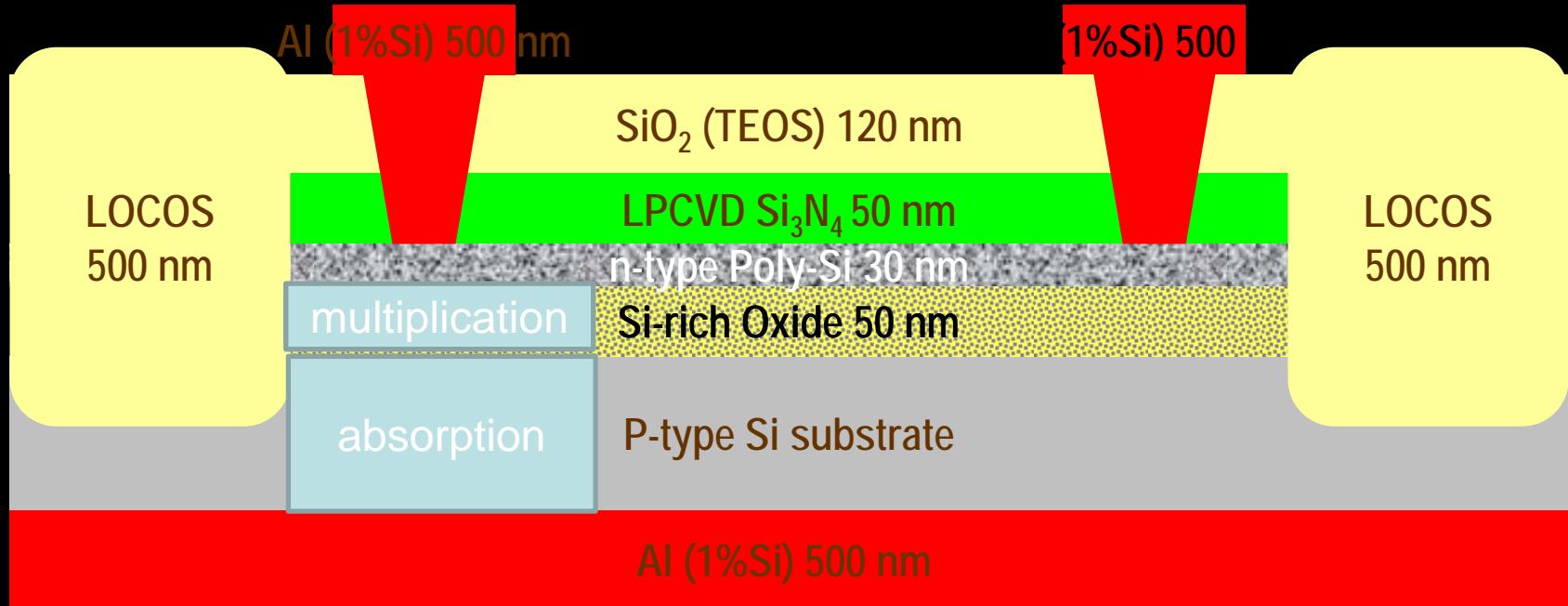
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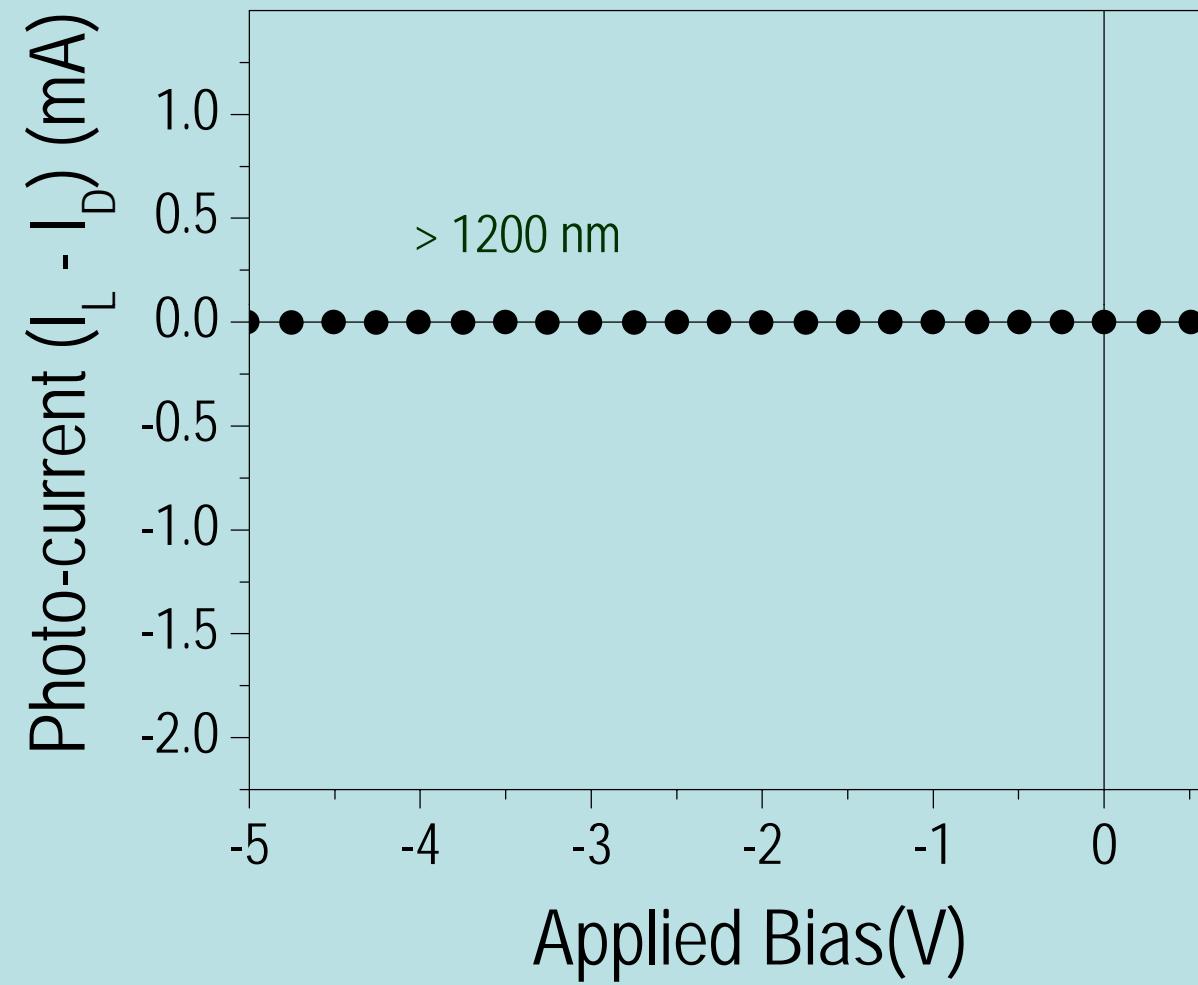
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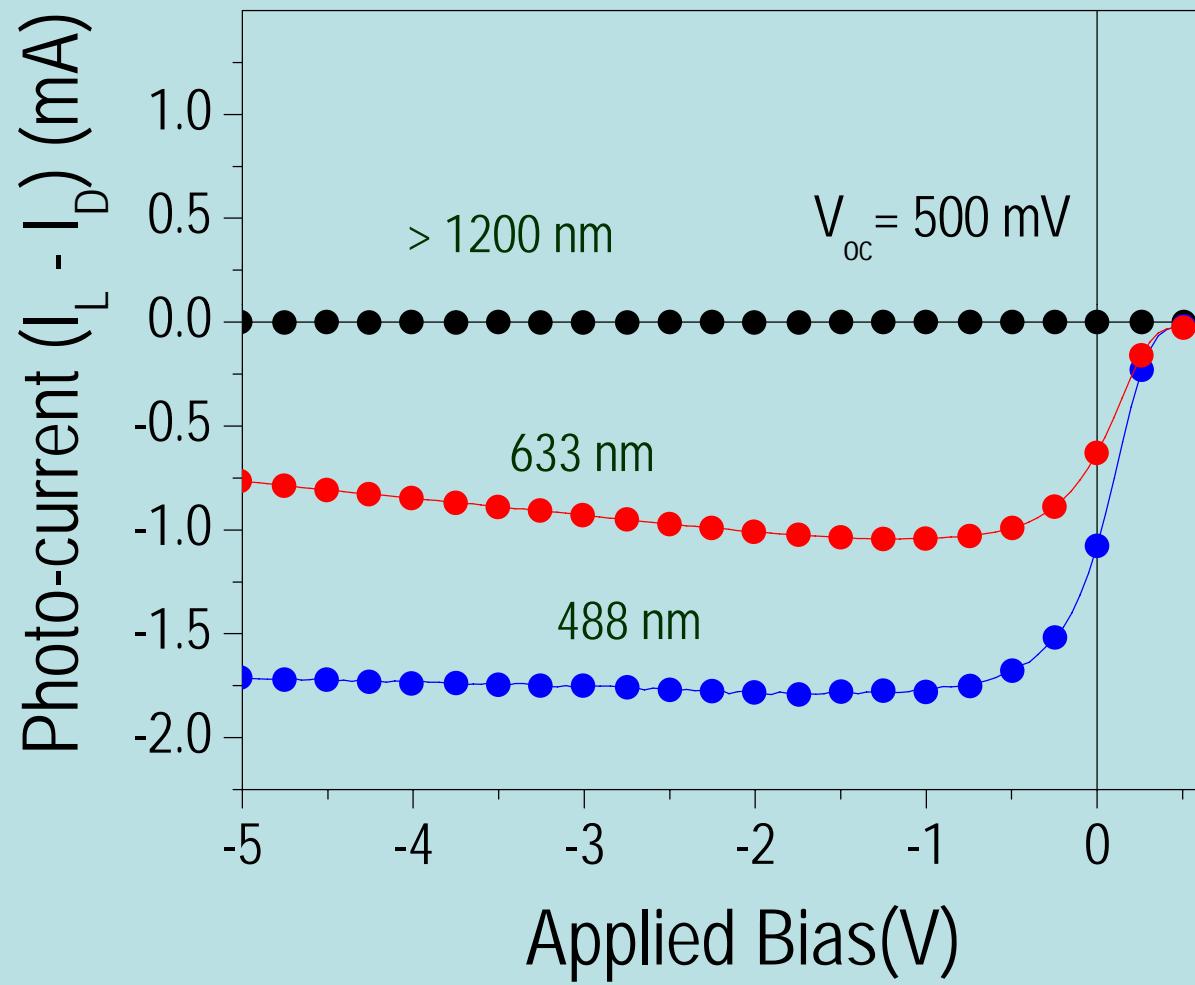
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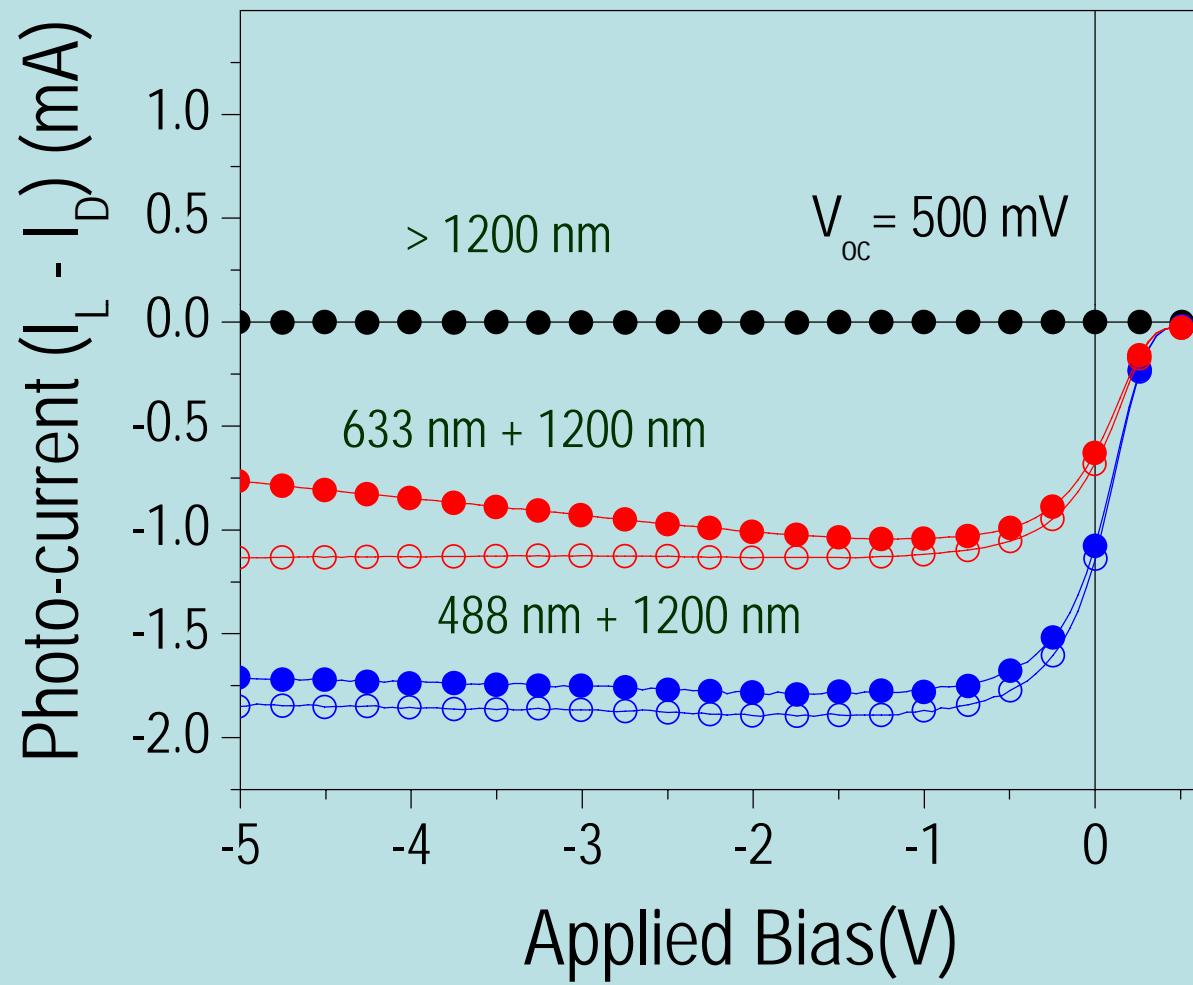
# IR response in $\Gamma$ 3N



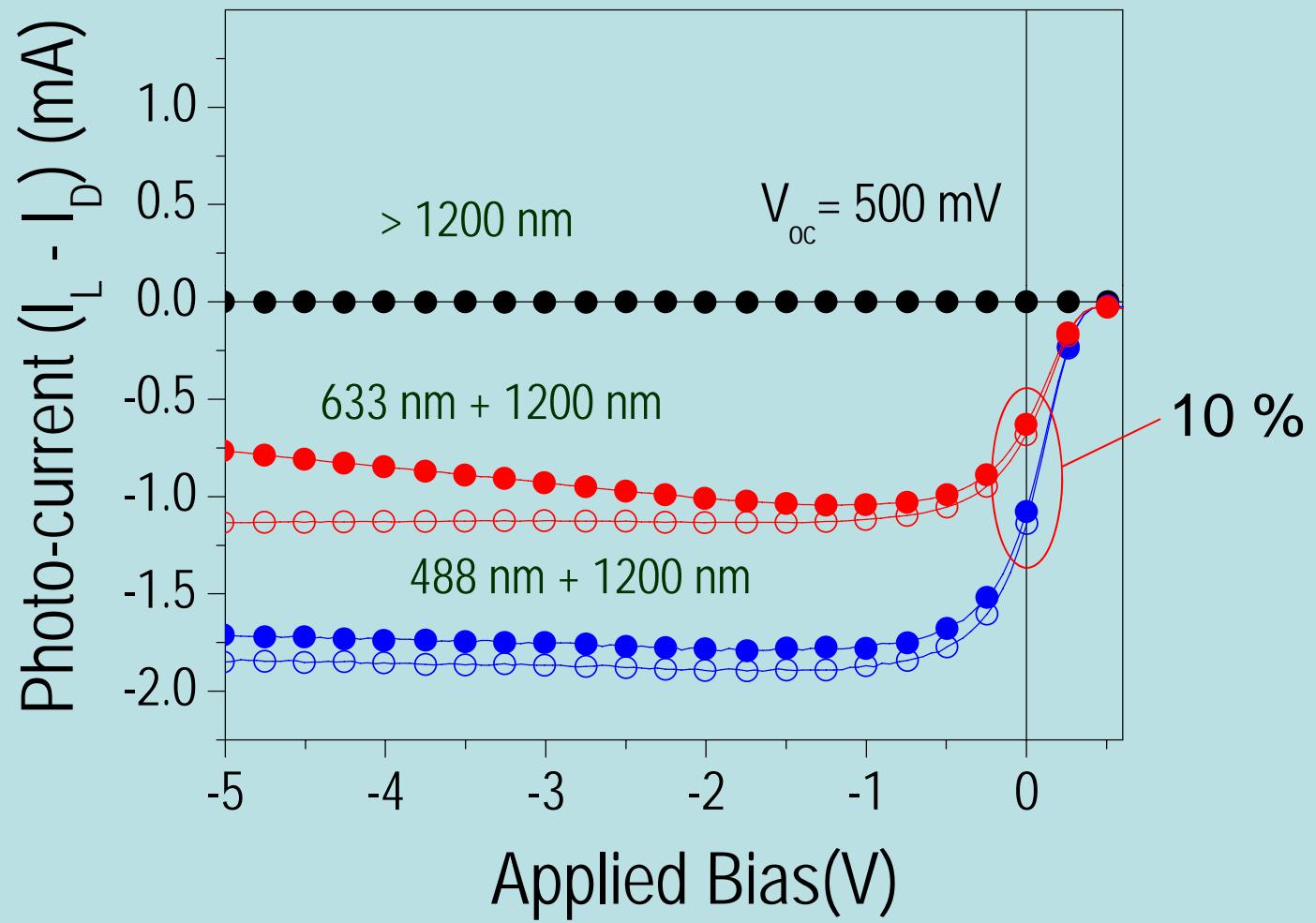
# IR response in $\Gamma$ 3N



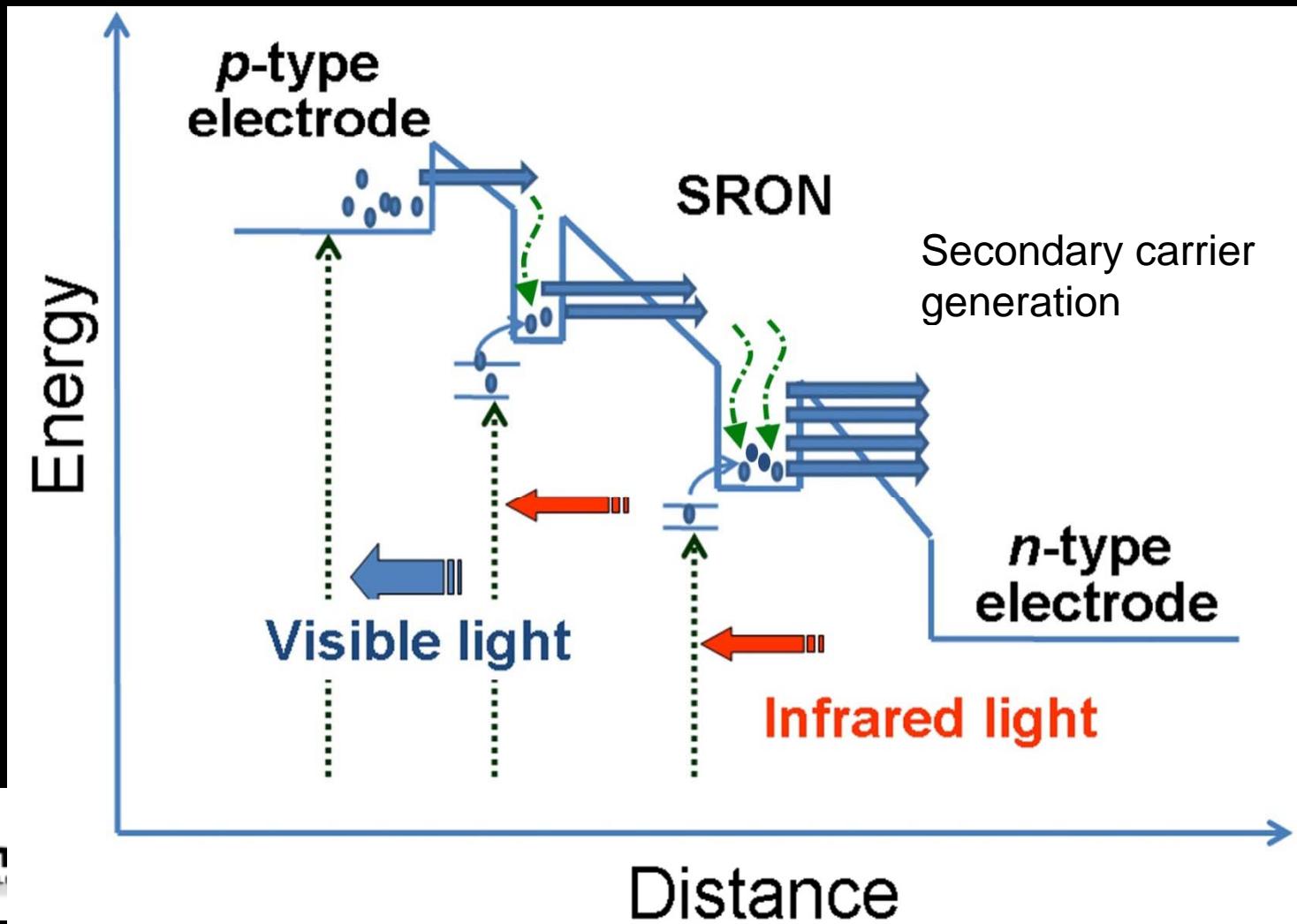
# IR response in $\Gamma$ 3N



# IR response in $\Gamma$ 3N



# Solar cell with an internal gain mechanism



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# Outline

- Silicon Photonics
- State of the art
- Silicon Photonics for lab-on-a-chip
- NanoSilicon photonics
- Conclusion



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# Conclusions:

- Silicon photonics is a mature technology
- Silicon photonics allows fabricating thousands of photonic components in a single chip
- Silicon photonics merges electronics and photonics to enable novel functionalities
- Silicon photonics is not only bulk Silicon (nanosilicon, strained silicon, silicon/germanium, germanium, ....)
- Silicon photonics is not only optical communication is much more



# Bottom line:

- Each time the market catches size  
Silicon is the solution
- If you may want to compete with silicon,  
do not! Silicon will always make it



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pHotonics ELectrronics functional  
Integration on CMOS

# Silicon photonics course

prepared by the HELIOS consortium

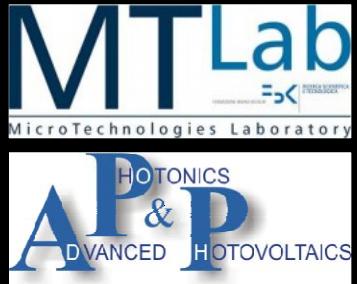
Download the course on <http://www.helios-project.eu/Download/Silicon-photonics-course>



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# Acknowledgments



- EC: Helios, LIMA, Wadimos, Positive
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- MAE: Italy-turkey, mexico, romania
- HCSC project and Optol
- ITPAR



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